



# Technoprobe S.p.A. Company Presentation

May, 2026



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# Innovation begins with us

A leading company in the field of semiconductors and microelectronics



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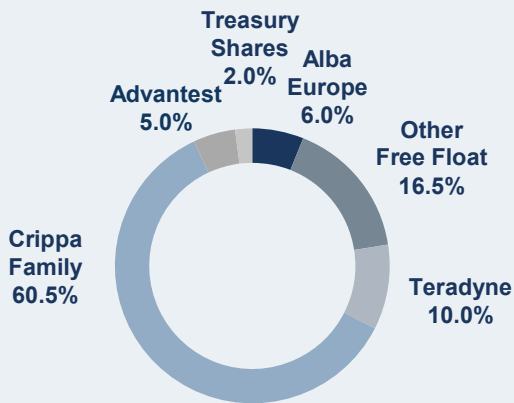
# Company Overview



## 2025 Key financial metrics

Revenue	Ebitda	Net Income	Net Financial Position	Mkt Cap
<b>€628.4m</b> <b>+16%</b> YoY	<b>€201.4m</b> <b>32%</b> EBITDA margin	<b>€98.8m</b> <b>16%</b> on revenues	<b>€684.2m</b> as at 12/31/2025	<b>~€18,5bn</b> as at 5/18/2026

## Shareholding Structure



- 

Leading player in designing and manufacturing of **probe cards to test Logic chips**
- 

Manufacturing process **vertical integrated**
- 

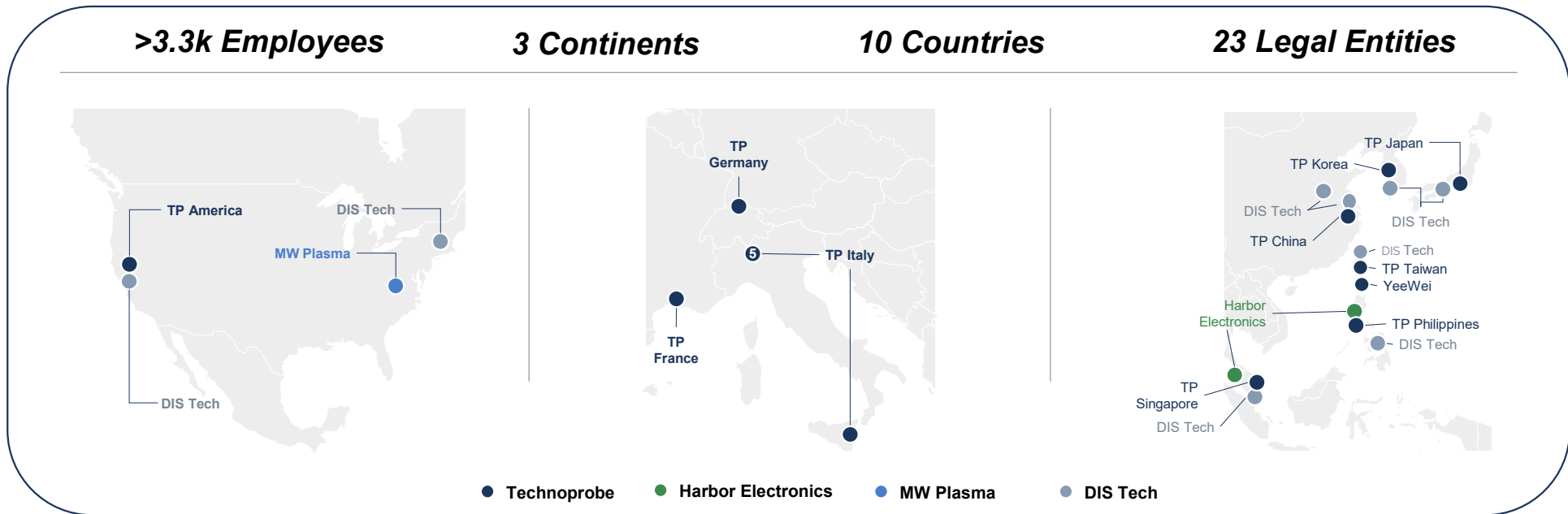
Strong focus on **innovation**
- 

Extensive **global presence** and widespread **local footprint**



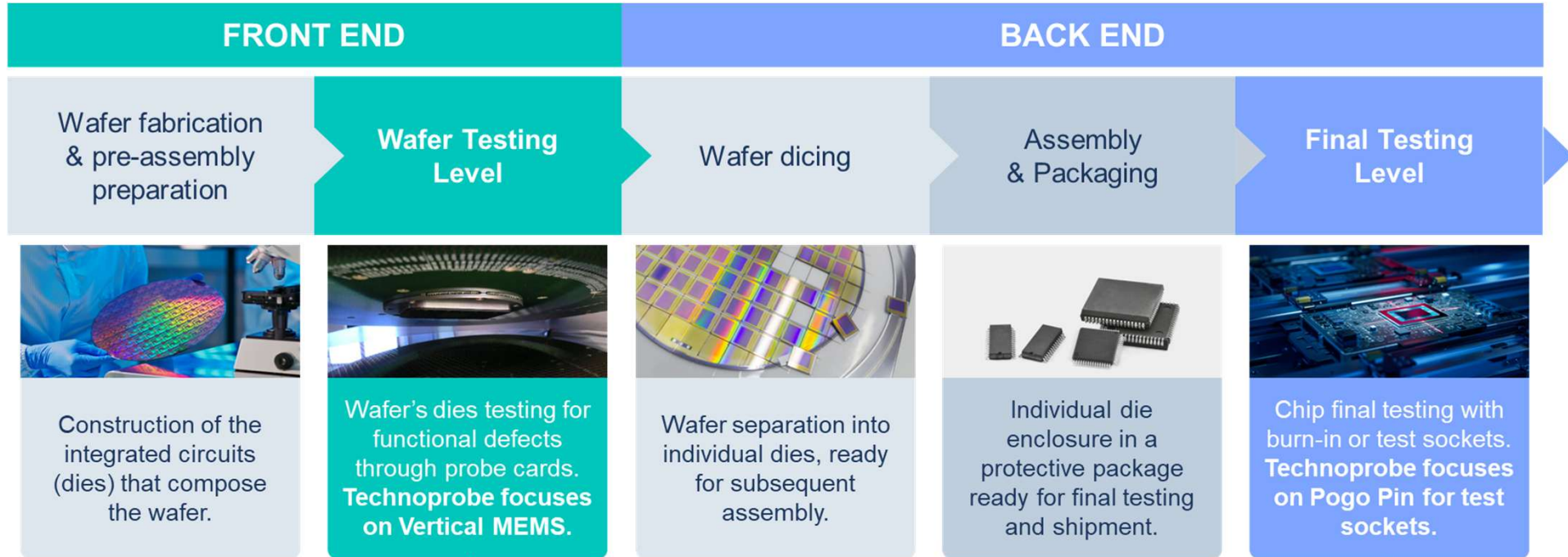
# Where we are

Headquartered in Italy with branches in Europe, America, and Asia



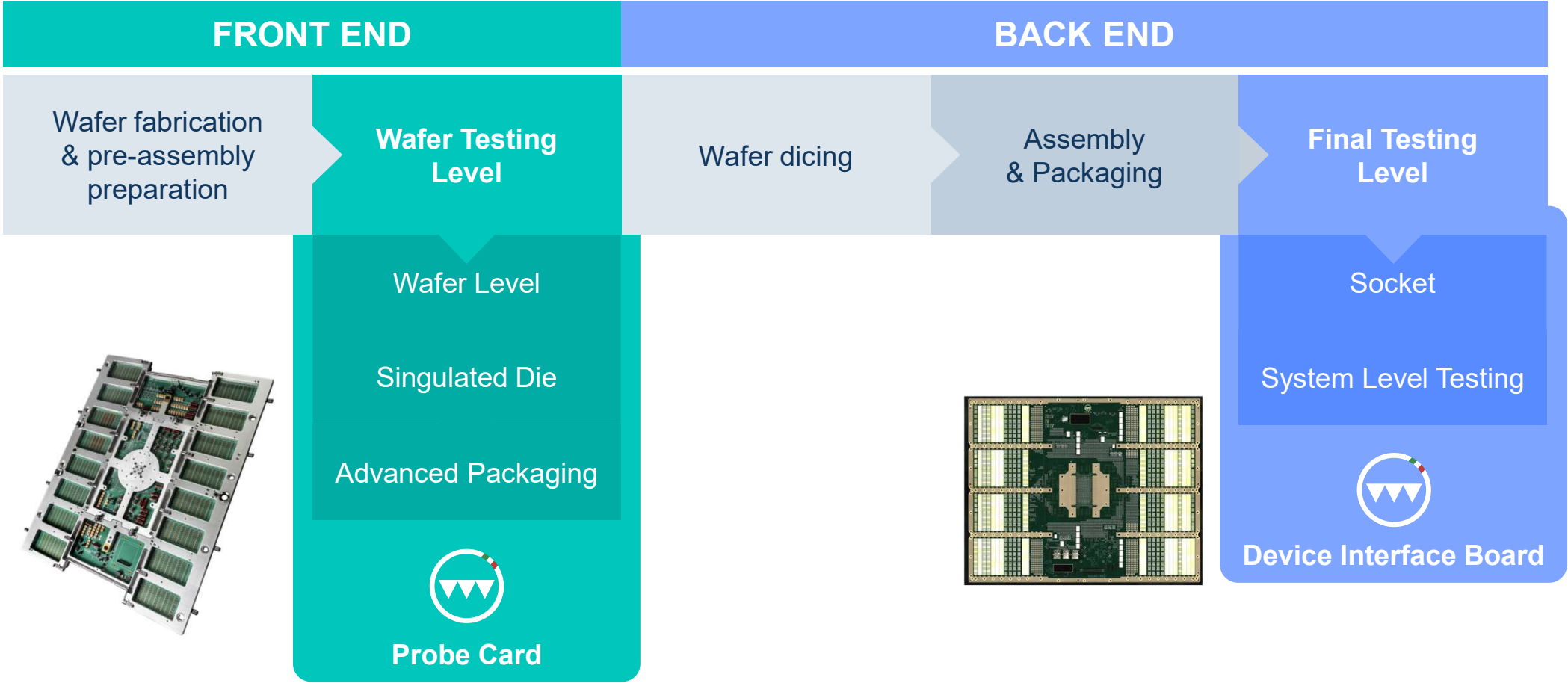


# Testing in the semiconductor manufacturing process



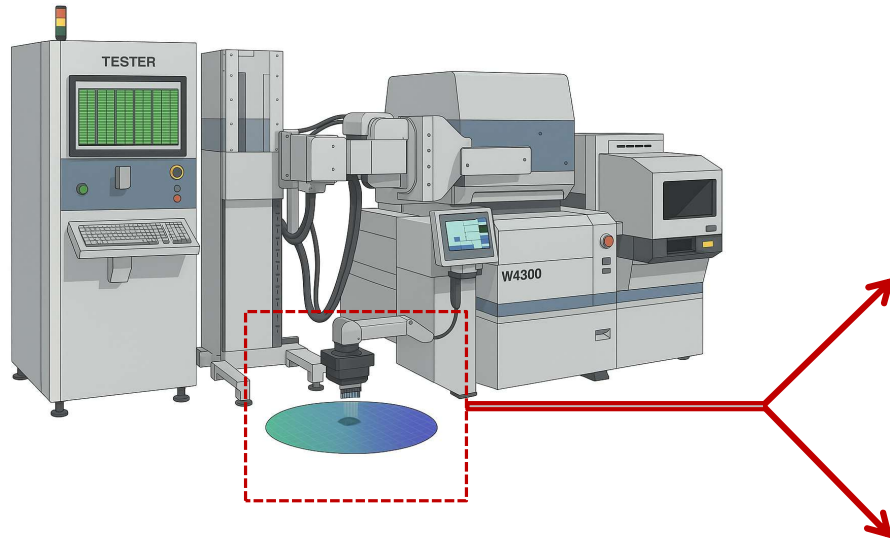


# Our positioning in the testing space





# The testing phase



## Tester (ATE)

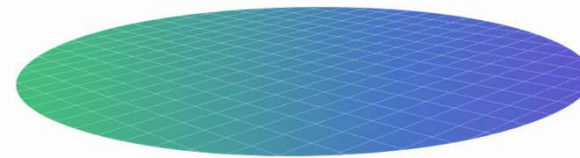
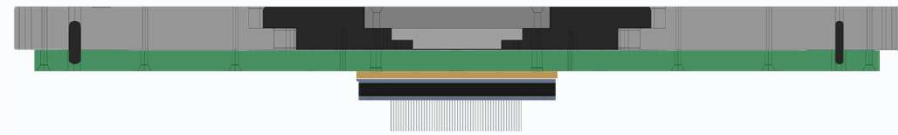
- A tester, or Automated Test Equipment (ATE), applies electrical signals to semiconductor devices and measures their responses to verify performance and functionality
- ATE systems execute test programs to identify manufacturing defects and ensure chips meet design specifications



## Probe Card



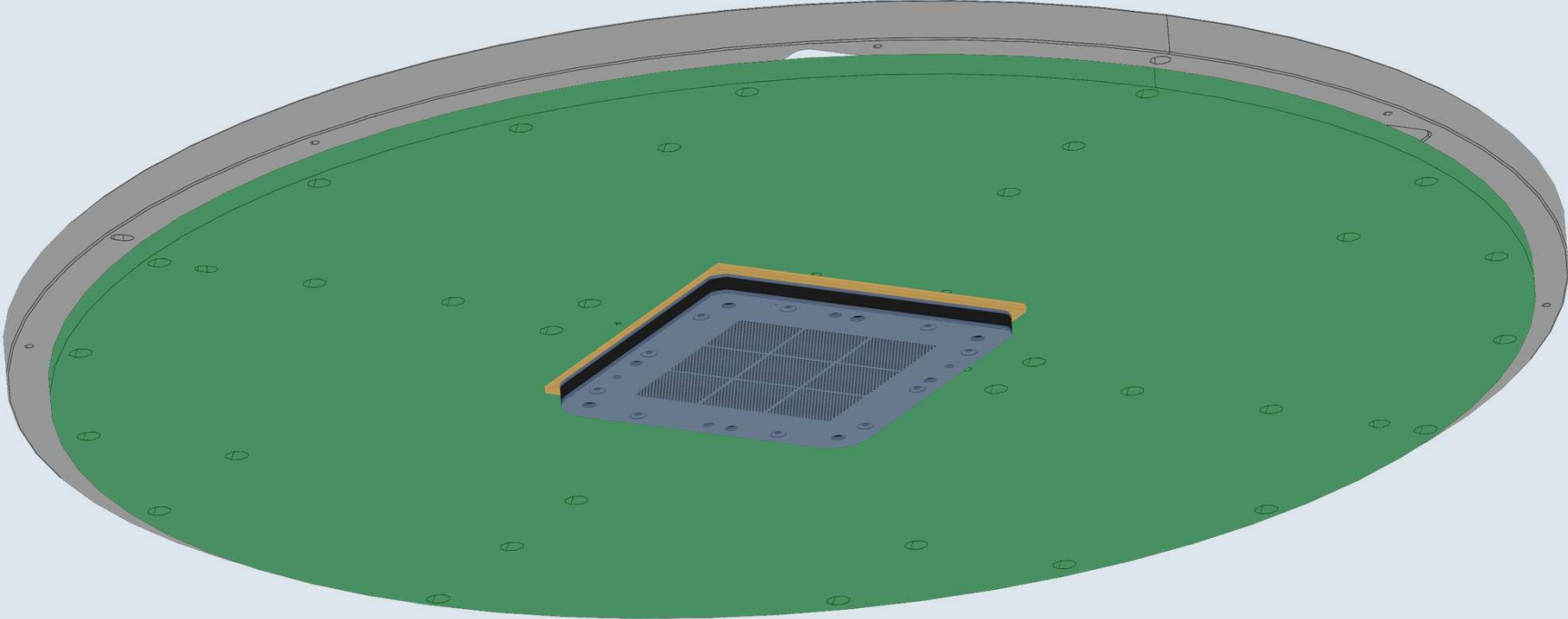
- A probe card is a precision device with microscopic needles or MEMS tips that make electrical contact with each die's test pads on the wafer
- The probe card interconnect a tester (ATE) with dies on a wafer or diced dies for electrical testing.



## Wafer

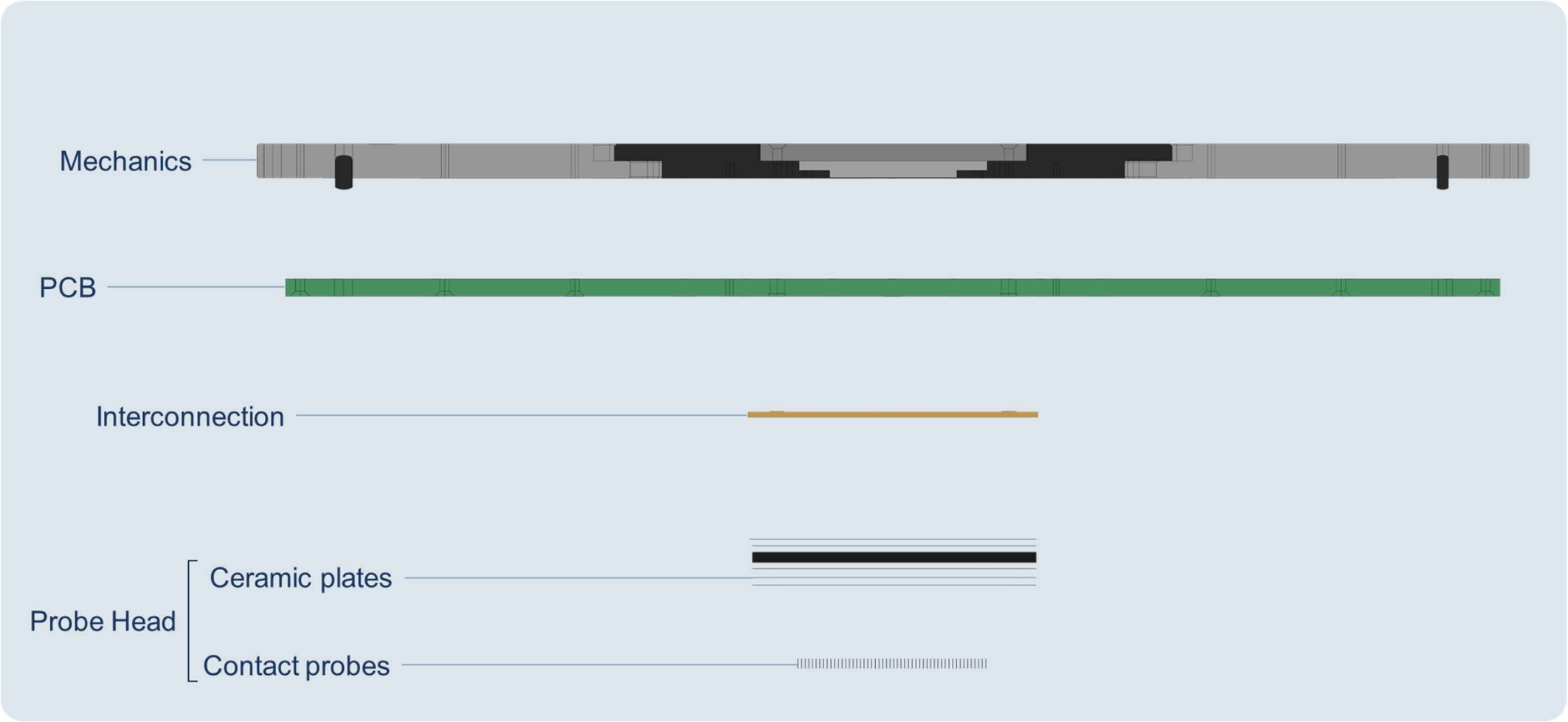
- A wafer is a thin, circular semiconductor substrate (most commonly silicon) on which integrated circuits (dies) are fabricated
- Each die functions as an individual integrated circuit that, once separated (diced) and packaged with external connectors, becomes a finished semiconductor chip

# The Probe Card





# The Probe Card





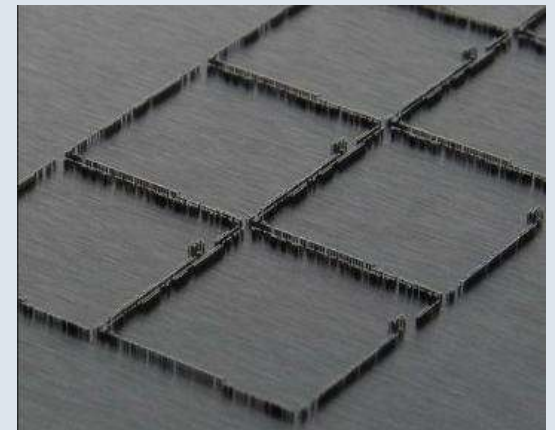
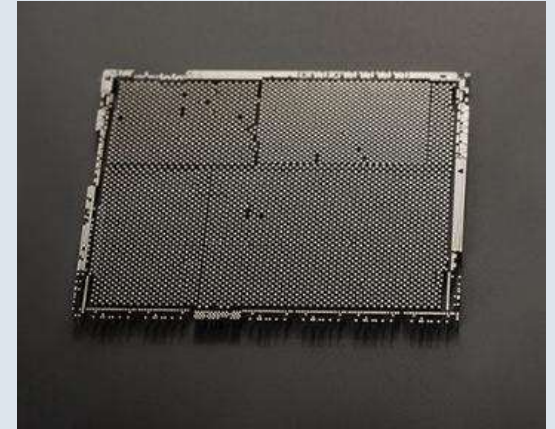
# The Probe Card

## Facts Sheet

1 probe card

100000+	Number of contacts interconnecting tester with device
1000A+	Ampere of currents to supply the device
20 $\mu$ m	Pad pitch to ATE space transformation of a factor >10x
100W+	Watts of power to dissipate through the card
200Kg+	Withstand a force of hundred kilograms
-60°C / +175°C	Wide supported operation temperature range

All requirements satisfied within a 10cm x 10cm x 1cm 3D space





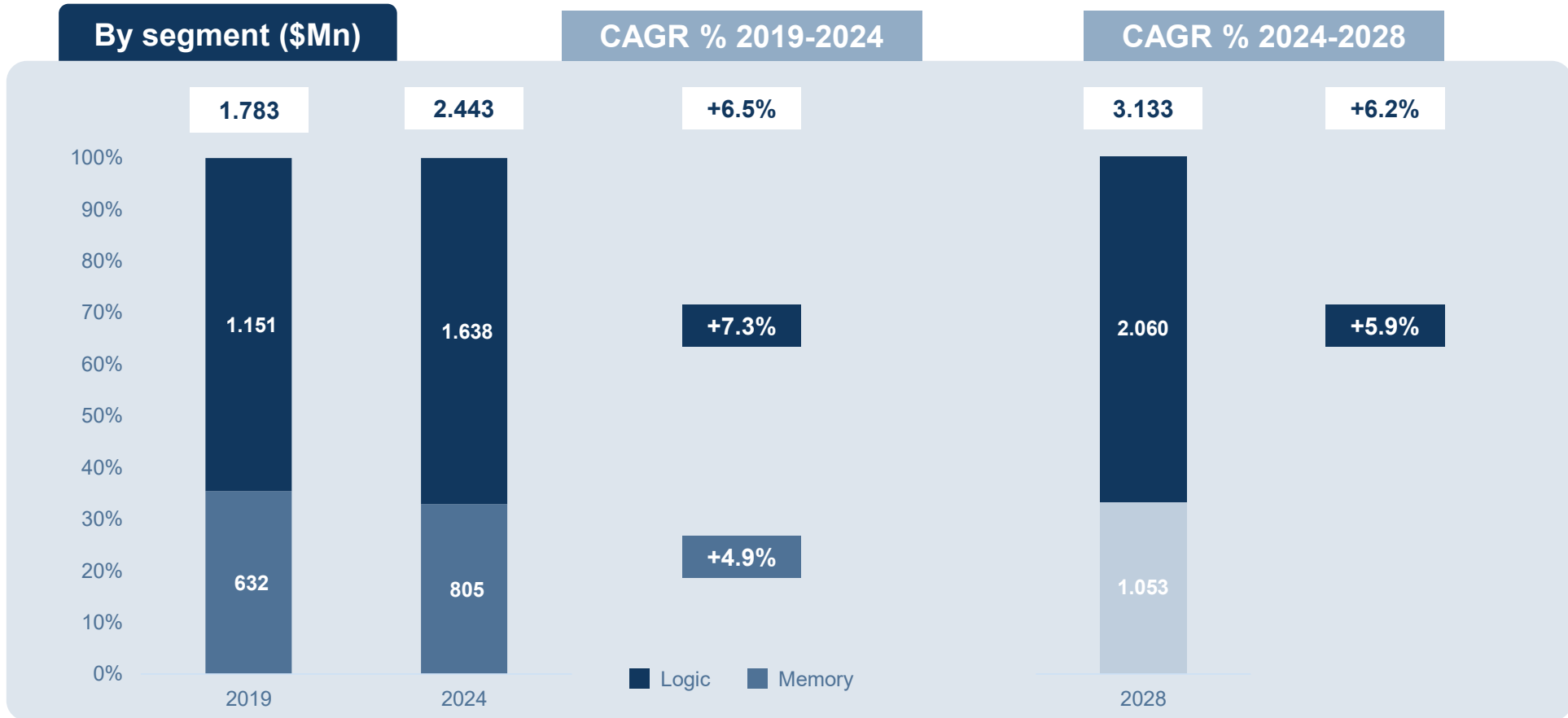
# Reference Market



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# Overview of the Semiconductor Probe Cards market

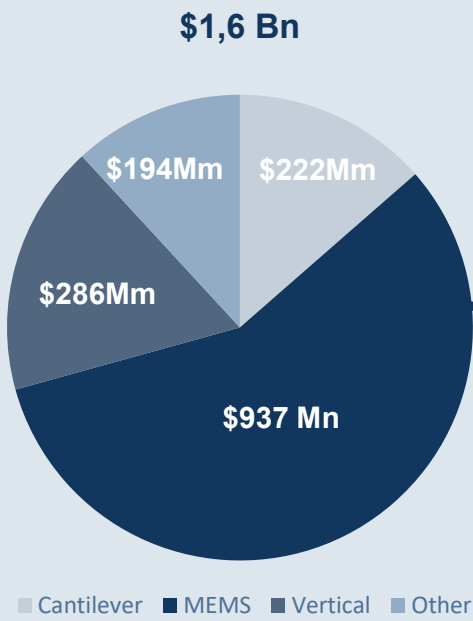


Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept. 2024) – rounded figures. Memory: DRAM+NVM & Other memory. Logic: MEMS, Power, RF, CMOS Image Sensors, Photonics, Other non-memory, WAT.



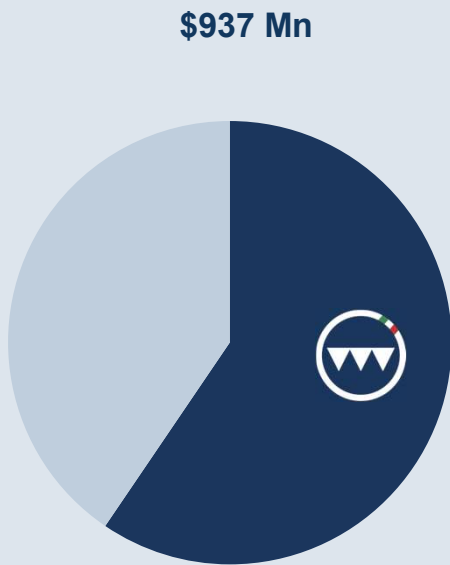
# Our reference market

2024 Logic Probe Card market



**Market Share: 34%**

2024 MEMS Logic Probe Card

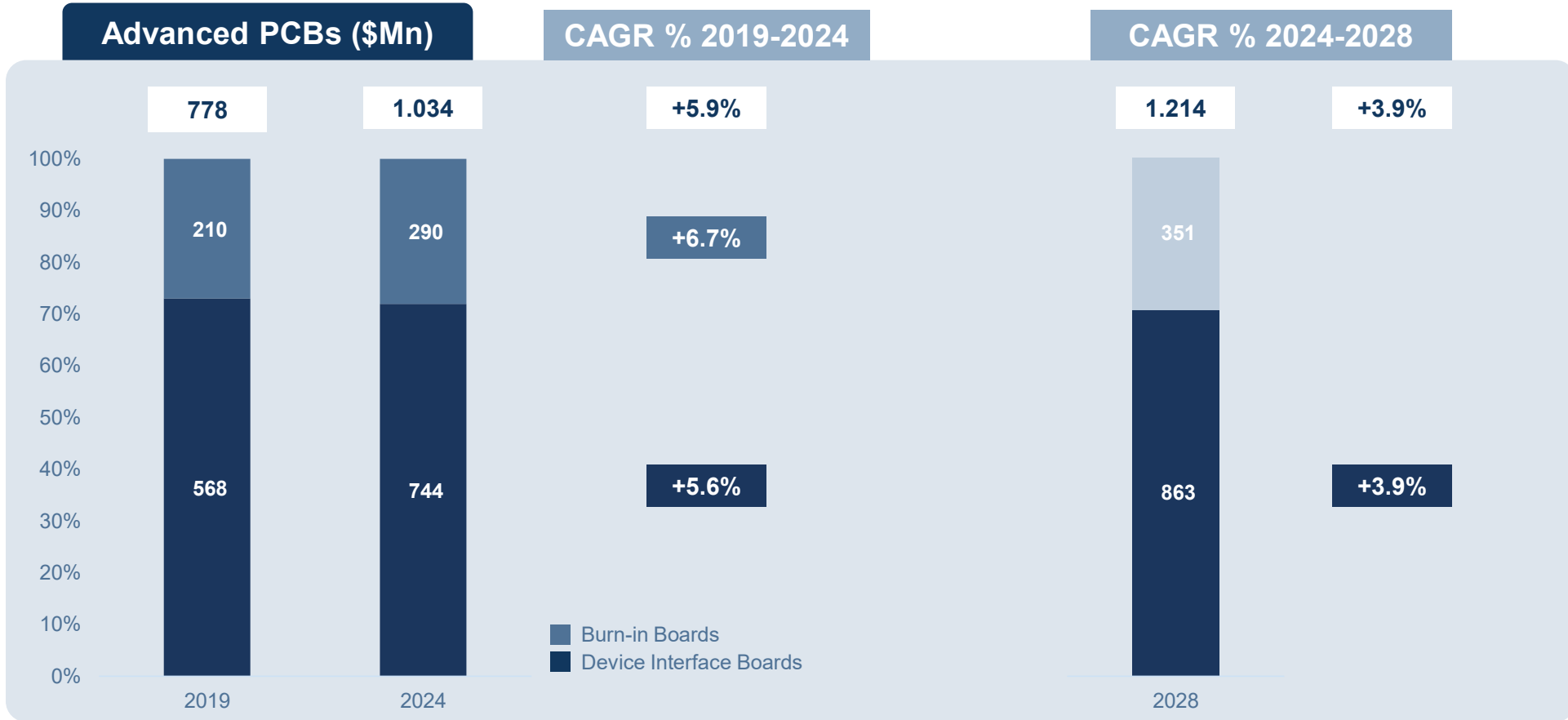


**Market Share: 60%**

Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.



# Final Testing market – Advanced PCBs



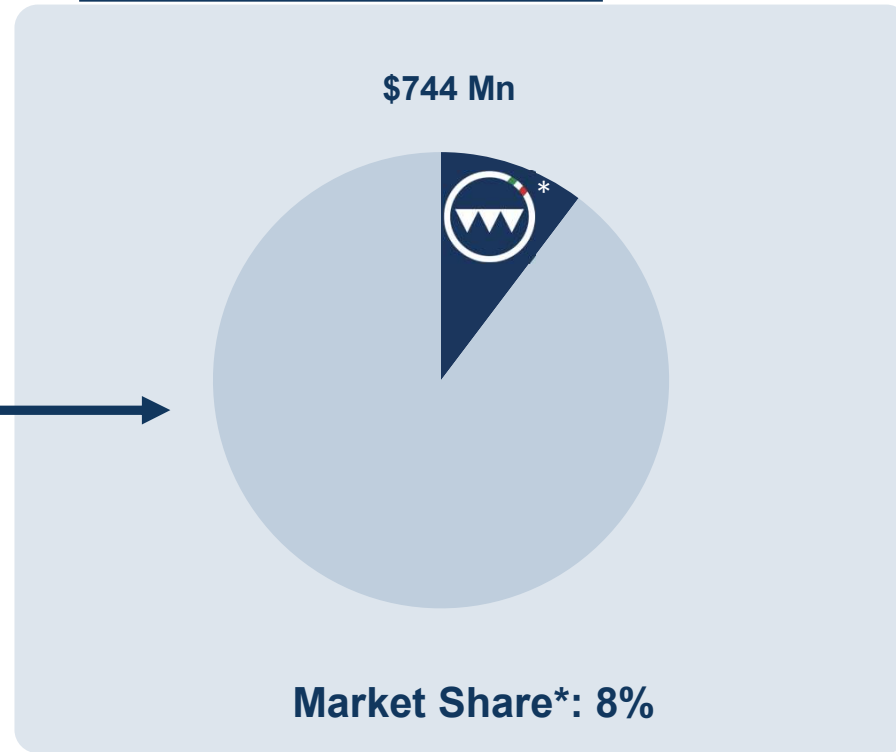
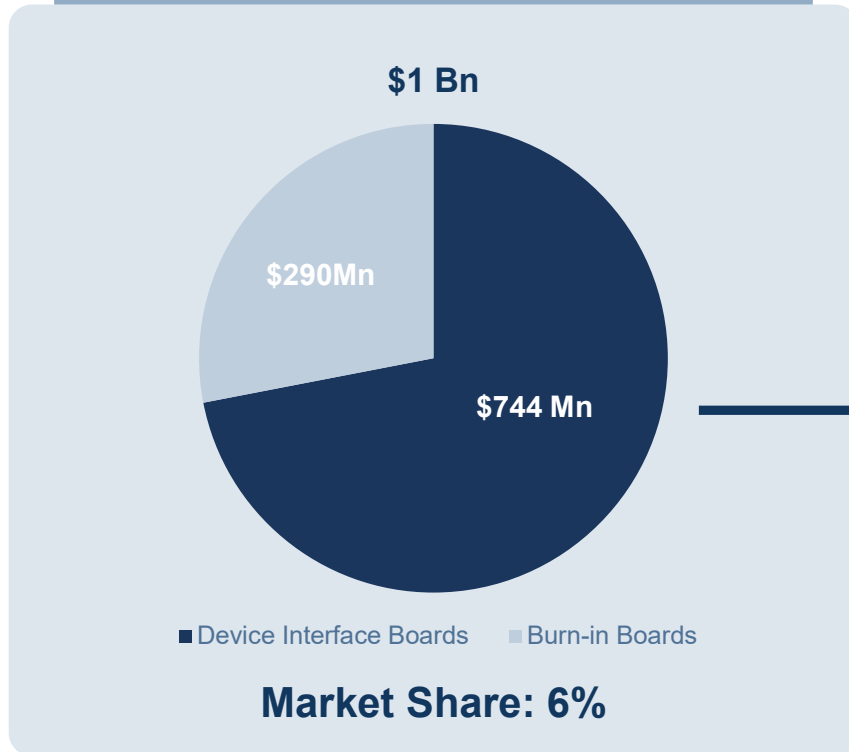
Source: Yole Test Interface Board market monitor Q3 2024 (Sept. 2024) – rounded figures.



# Final Testing market – Our reference market

2024 Advanced PCB for semiconductor

2024 Final Test DIB market



Source: Yole Test Interface Board market monitor Q3 2024 (Sept. 2024) – rounded figures.  
(\* ) Based on DIS Tech Final Test FY24 data. Company acquired by Technoprobe on May 27, 2024.



# Business Model



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# A successful and vertically integrated business model



# Supported by an open eco-system partnerships



## TERADYNE

**Accelerate growth** of complete Probe Card and Final Test Interfaces by acquisition of DIS

**Joint Development Projects** to deliver superior customer value in SOC and Memory



## TECHNOPROBE

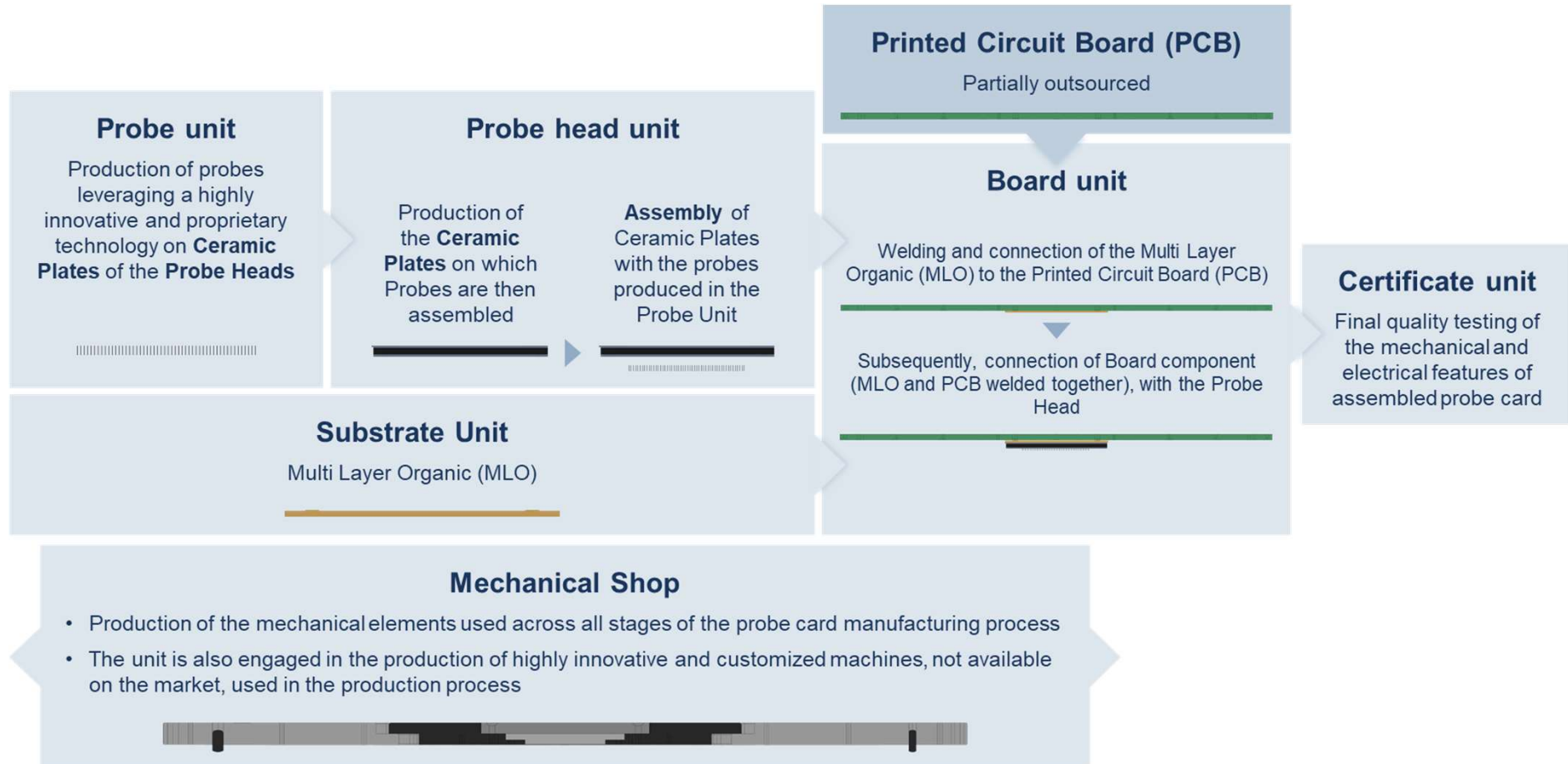
## ADVANTEST

**Priority suppliers** of PCB

**Joint Development Projects** to share knowledge



# The Probe Card manufacturing process

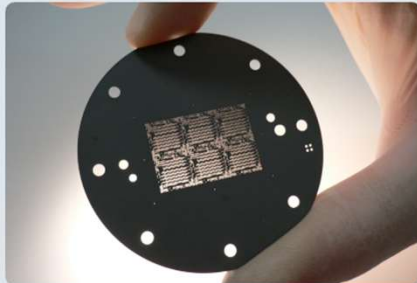




# A wide range of highly innovative technologies inside

## Advanced micromachining

Advanced laser cutting:  
high accuracy and fast lead time



## Thin film

Strong investment in advanced thin film technology to reduce lead time and improve quality and complexity



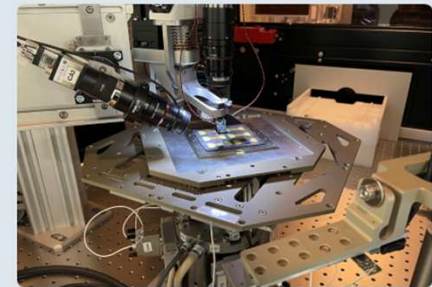
## 3D MEMS

Acquisition of MICROFABRICA in 2019; the sole company in the world specialized in 3D metallic MEMS manufacturing



## Advanced manufacturing

Advanced manufacturing for high volume and best quality assembly of micro components





# Vision & Strategy



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# Challenges & strategic setting

**1** **Evolution of chip technology**  
(more than Moore)  
Scaling slow down as enabler for **chiplets**,  
**3D architectures** and **new materials**

- **Continuous investments in R&D**
- **M&A as accelerator of technological development**

**2** **Increase in complexity**  
**Design and manufacturing** are becoming essential capabilities to reliably deliver **complex solutions**

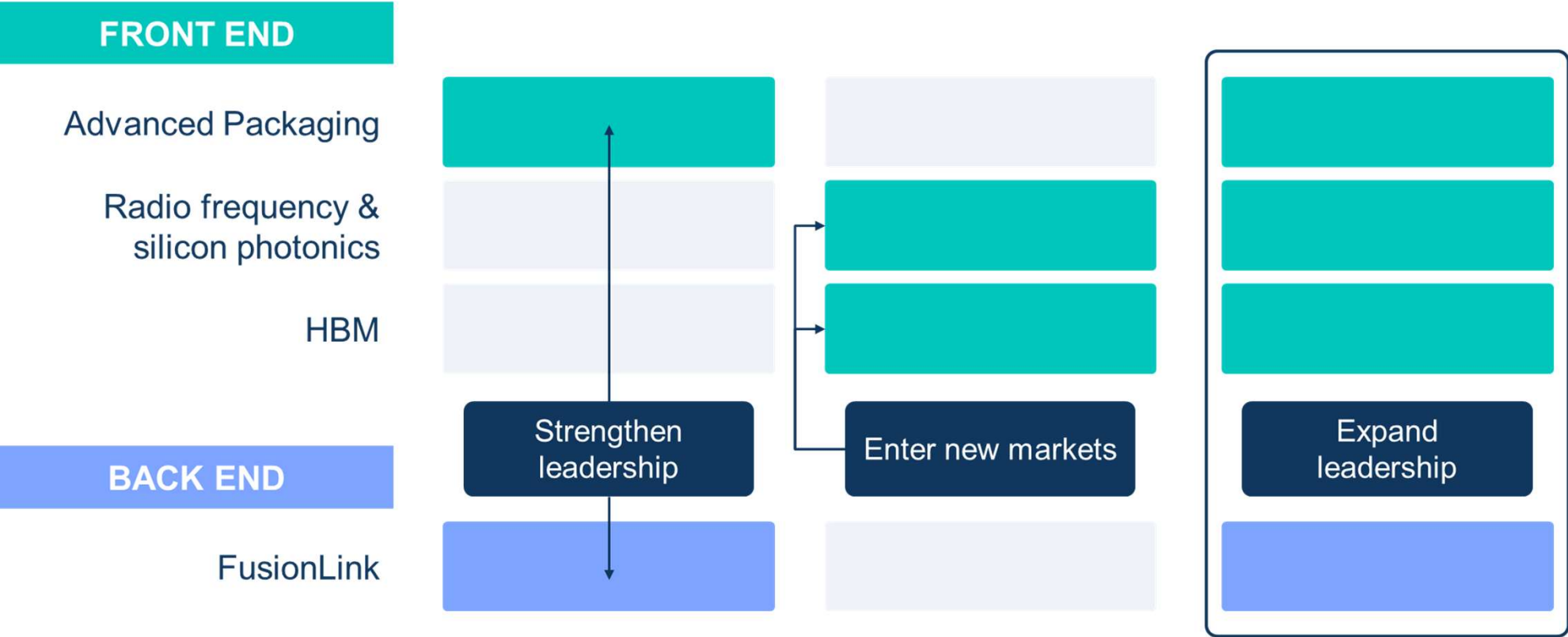
- **Strategic partnerships**
- **Vertical integration of the most value-added components of the probe card**

**3** **Client satisfaction**  
Reliability of the product & **on-time delivery**

- **Support on site**
- **Commercial agreements**



# Growth drivers & trajectories

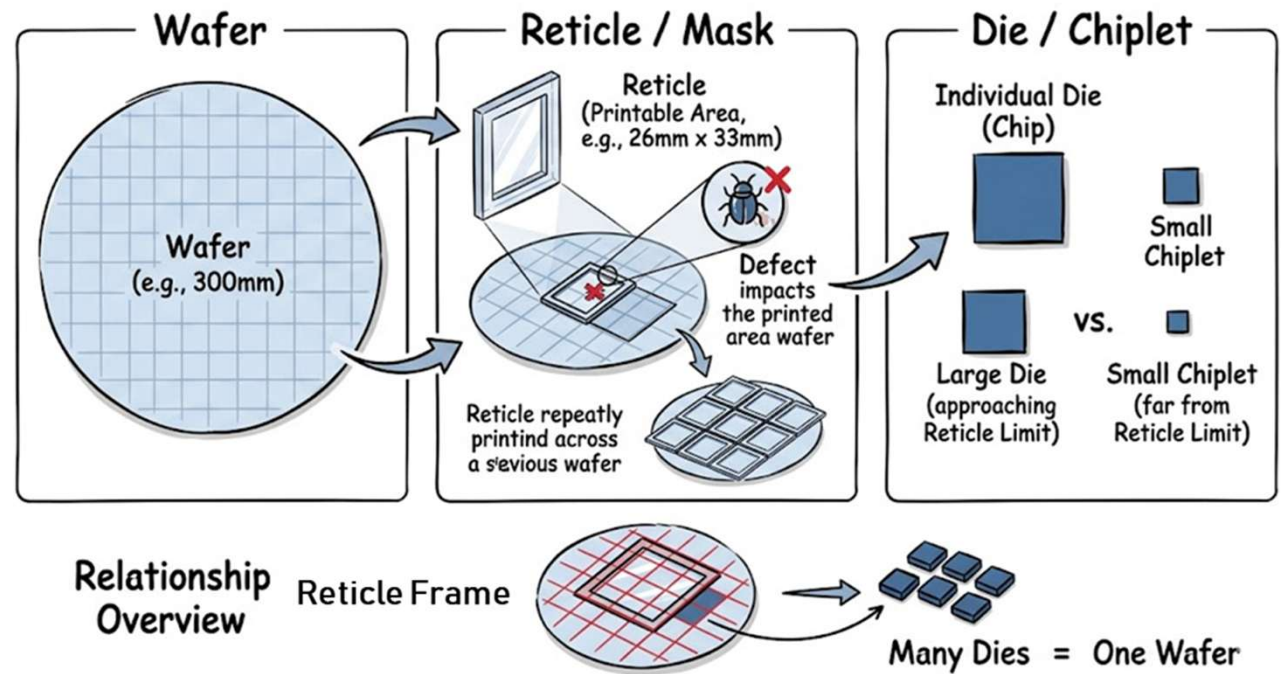




# Advanced Packaging: Yield Motivations

**The Reticle:** maximum area printable by lithography machine (~ **26mm x 33mm**). You **cannot** manufacture a chip larger than this “frame”.

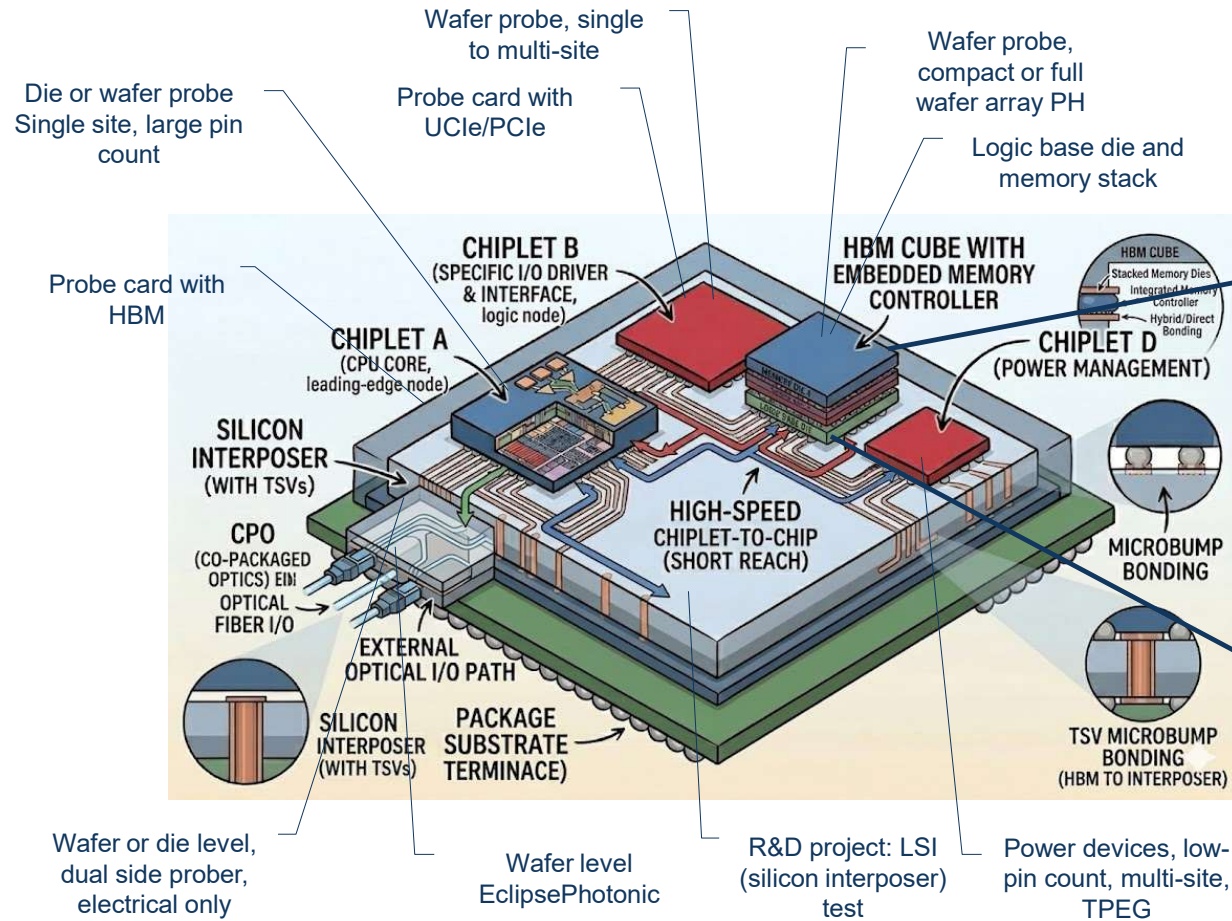
**The Solution:** AP bypasses the reticle limit by "stitching" **high-yield chiplets** together to create a system that functions one ultra-powerful chip.





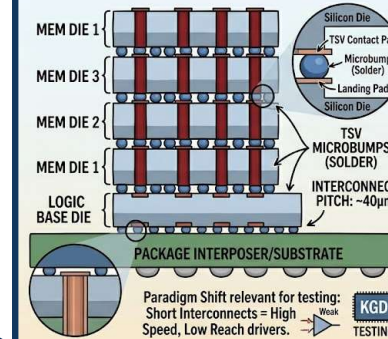
# Typical processor architecture

## WHERE OUR PROBE CARDS PLAYS

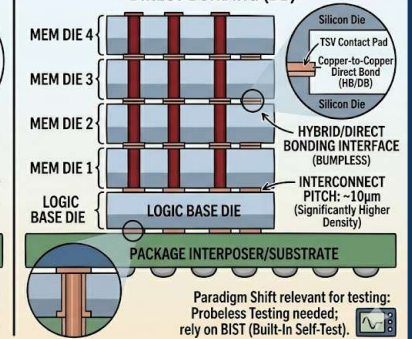


### 3D STACKED INTERCONNECTS: HBM (HIGH-BANDWIDTH MEMORY) EVOLUTION

Panel A: HBM with MICROBUMP BONDING



Panel B: HBM with HYBRID BONDING (HB) / DIRECT BONDING (DB)





# Technoprobe as advanced packaging enabler

**Fine pitch and ultra – large pin count**  
Necessary to effectively probe HPC and HBM's and all leading-edge product

**High-speed**  
Short, ultra short and RF-specific needles technology to manage high speed interconnect IO, including SiPho



- High power and thermal**
- Delivering high power to DUT in effective and reliable way
  - Ability to remove heat dissipated by the probe card (directly or because of power transferred from DUT to PC)

**High-density interconnect**  
Ultra-high complexity PCB and MLO/MLC for resource fan-out on ATE/SLT



# A hungry world of wideband applications



Exponential increase in number & type of connected things



Increasing reliance on the cloud



Bandwidth-hungry applications

## Analog radio frequency

Satellite communications and sensing, automotive radar, mobile communication,...



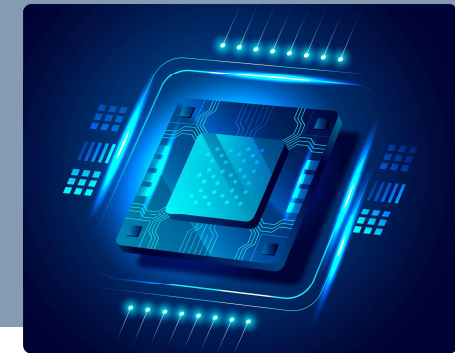
## Chiplet probing

High density and high-speed IO inside chiplet demand for high-performance probe needles



## Silicon photonics

Chiplet to chiplet interconnect / photonics-driven computing

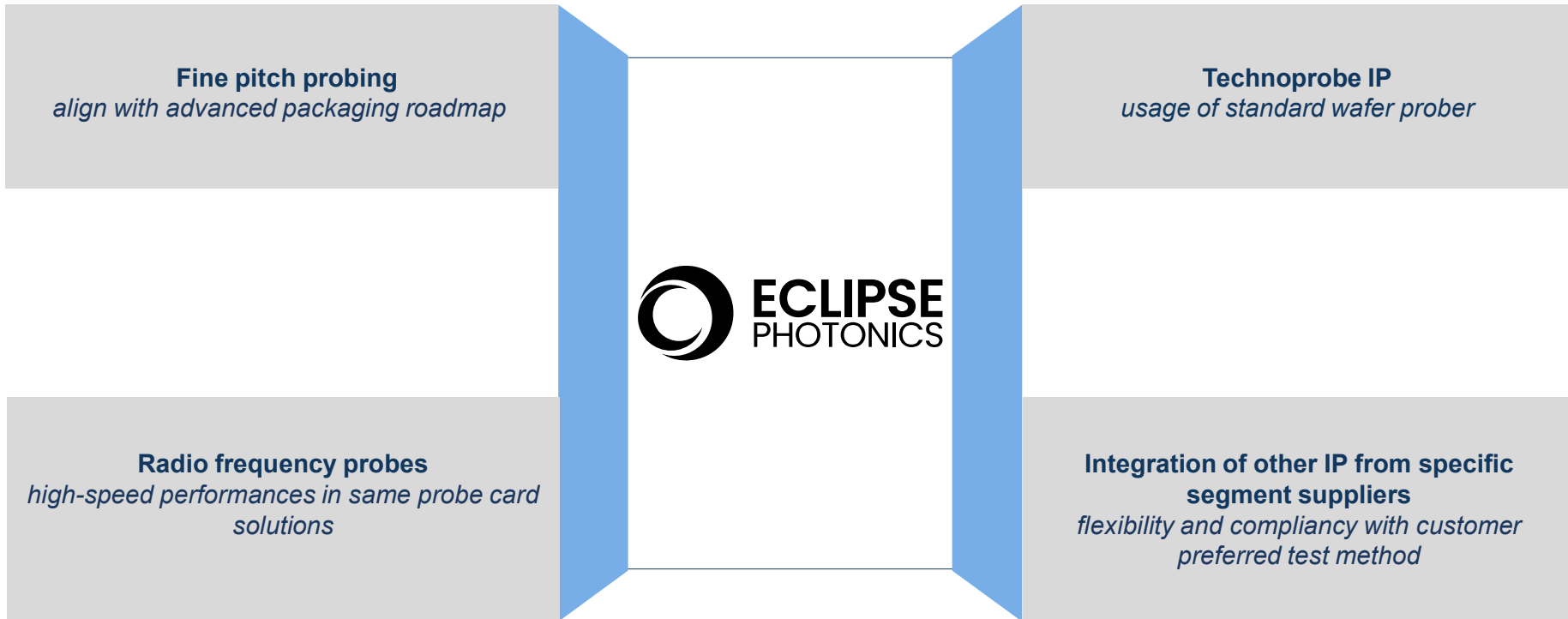


FRONT END Proliferate radio frequency and silicon photonics

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# Technoprobe silicon photonics testing solution



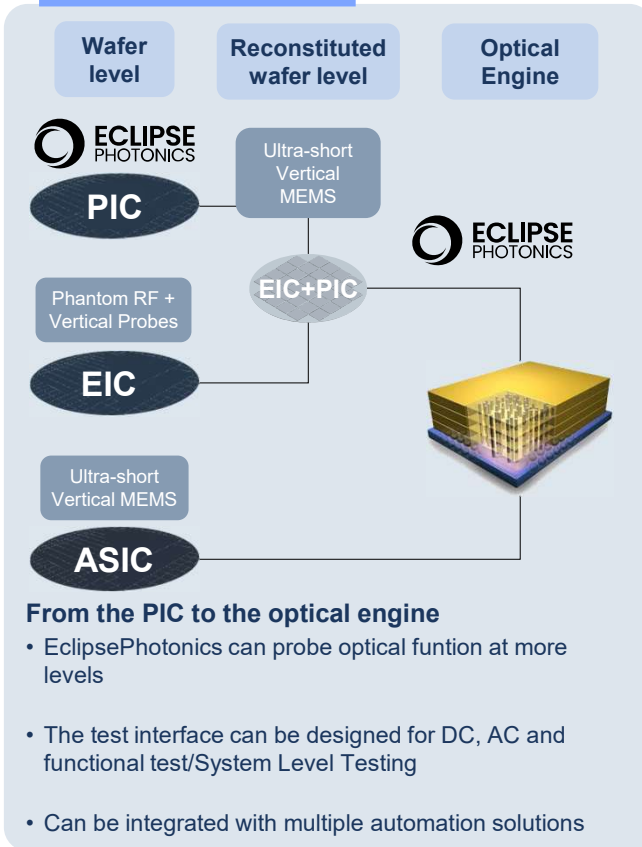
**FRONT END** Proliferate radio frequency and silicon photonics

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# Eclipse photonics

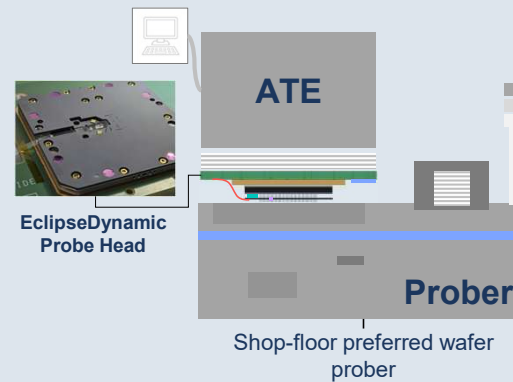
## Where it applies



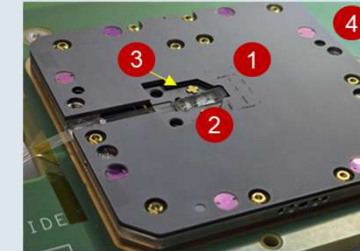
## How it works

### An autonomous instrument

- EclipsePhotonics embeds the electronics to autonomously operate when on the tester
- It integrate a programmable unit to execute the alignment algorithm(s), interface to the tester and operate the electronics
- The integration with ATE gives the capability to control the instrument from the user test program



## What it delivers



### Probe card content

1. Vertical MEMS needle and Phantom RF probes
2. FAU, fiber optics and optical connector (blind mated)
3. FAU positioner (up to 6-axis)
4. Electronics to activate and control the positioner

### What it delivers

- Direct docking
- Integrated optical and electrical probe, with off-line card certification
- High operation stability, repeatability and immunity to external factors
- In-field repairability
- Minimal optical to electrical pin distance constraints

**PIC:** photonics integrated circuit   **EIC:** electronic integrate circuit   **ASIC:** Application-Specific Integrated Circuit

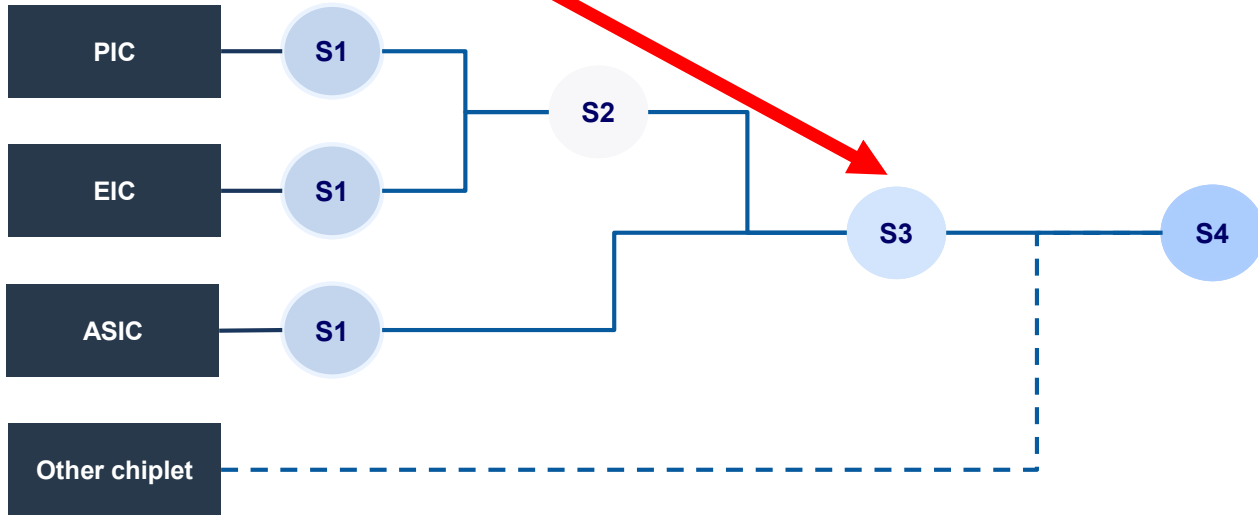
**FRONT END** Proliferate radio frequency and silicon photonics

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# Probe requirements

## MODELLING OF THE CPO TEST



Stage	PIC	EIC	ASIC
S1	O/DC	DC/AC	DC/AC
S2		DC	-
S3		O/DC/AC	
S4		ATE/SLT	

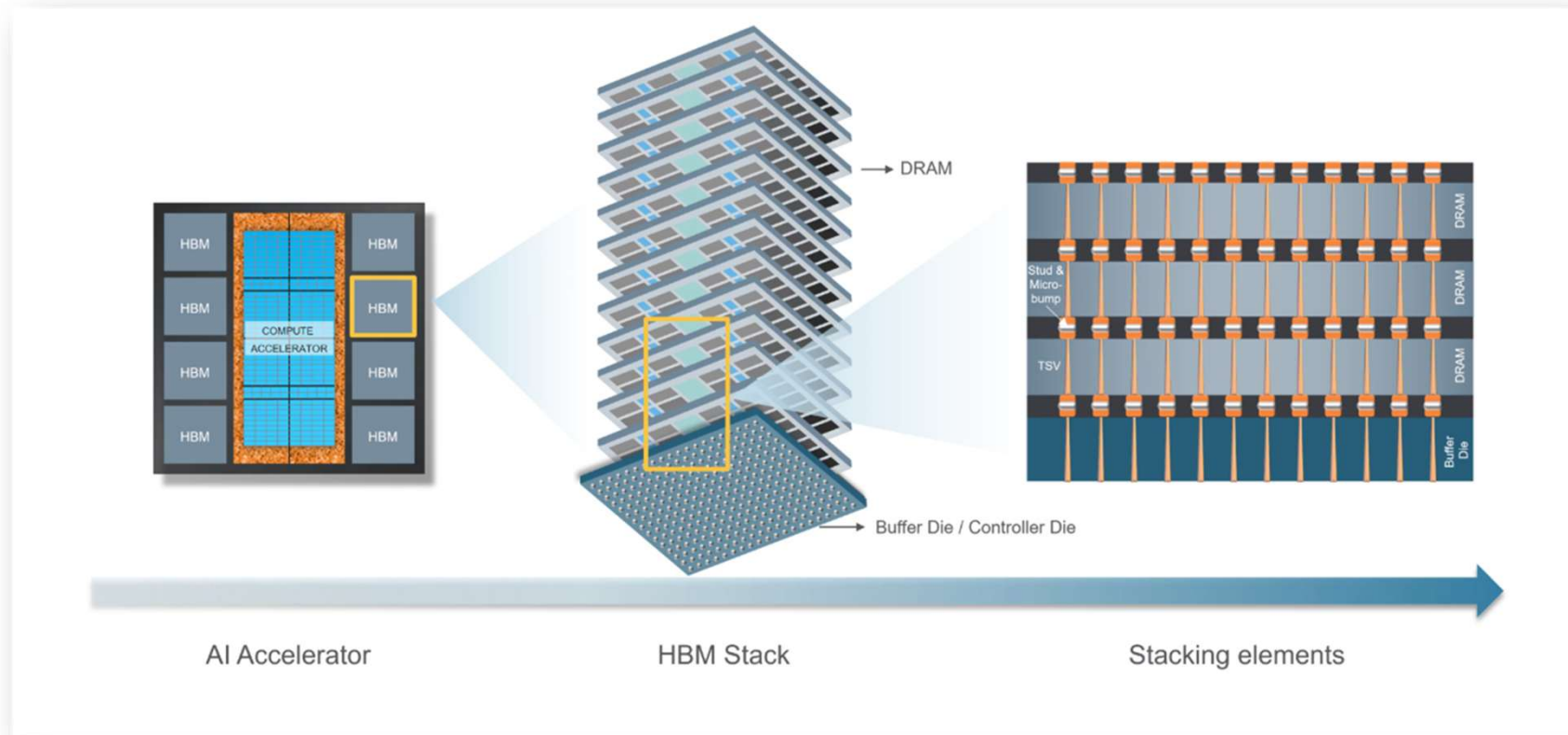
### Legenda

- O=Optical
- DC= DC test only
- AC= full perf. test including functional
- ATE= test using ATE
- SLT= mission mode test
- Note: AC may include RF test
- PIC: photonics integrated circuits
- EIC: electronics integrated circuits
- ASIC: Application-specific Integrated Circuits

FRONT END Proliferate radio frequency and silicon photonics

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# HBM Architecture



Cartoon credit: Applied Material web site

FRONT END Enter the High Bandwidth Memory (HBM) segment

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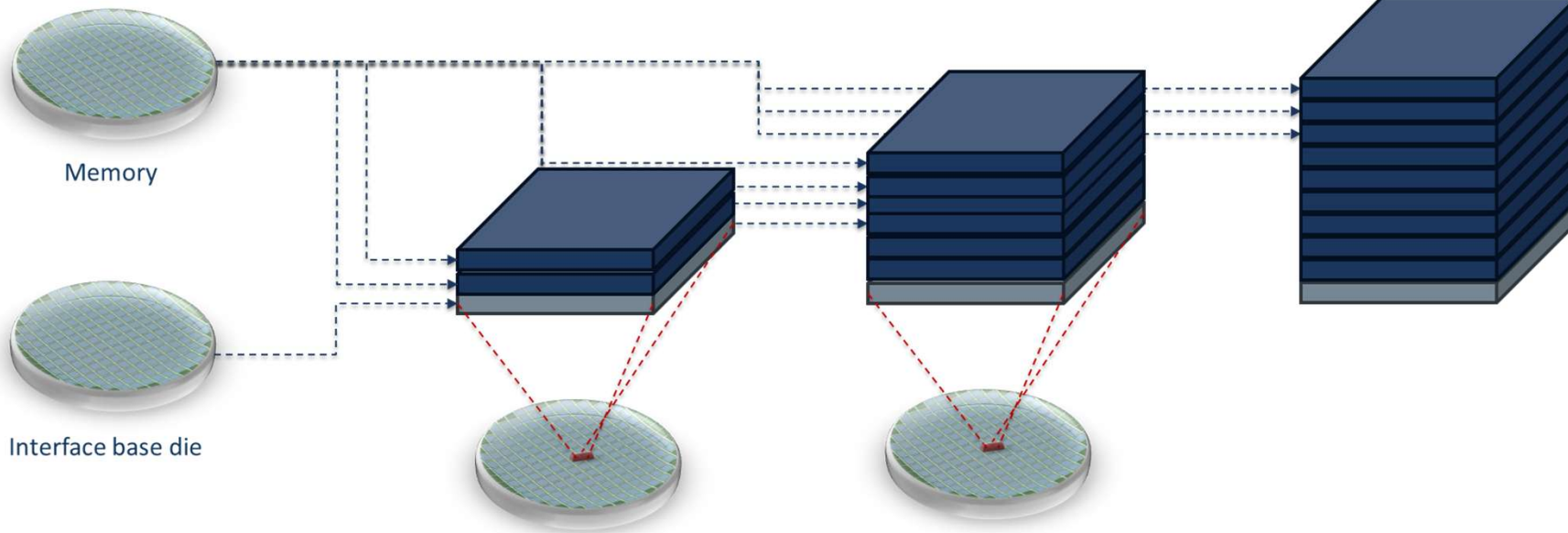


# HBM Test Flow

Wafer level

Intermediate ?  
Reconstituted wafer level

HBM cube  
Singulated Die level



Raw Defects

Interconnect

Interconnect

Performances

Logic  
Base die

Memory  
Sacrificial

Sacrificial

Sacrificial

FRONT END Enter the High Bandwidth Memory (HBM) segment

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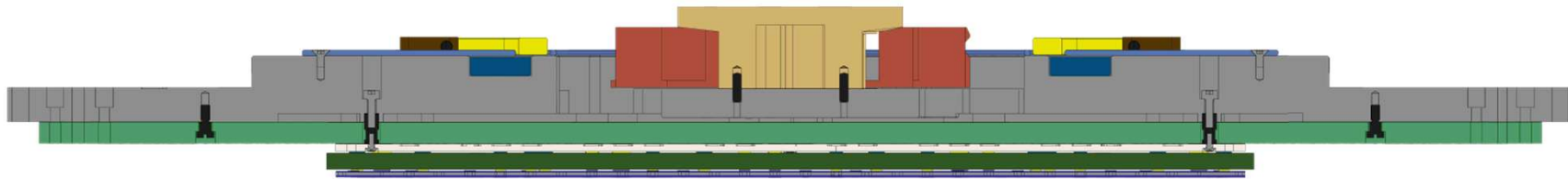


# HBM: new testing solution

DRAM and HBM are typically tested with **microcantilever** probing technologies.

Most **advanced HBM** and Next Generation products are becoming more challenging in terms of pad pitch, signal integrity, and power.

For both applications Technoprobe is leveraging on **Vertical MEMS** solution and on a unique PC architecture.



FRONT END Enter the High Bandwidth Memory (HBM) segment

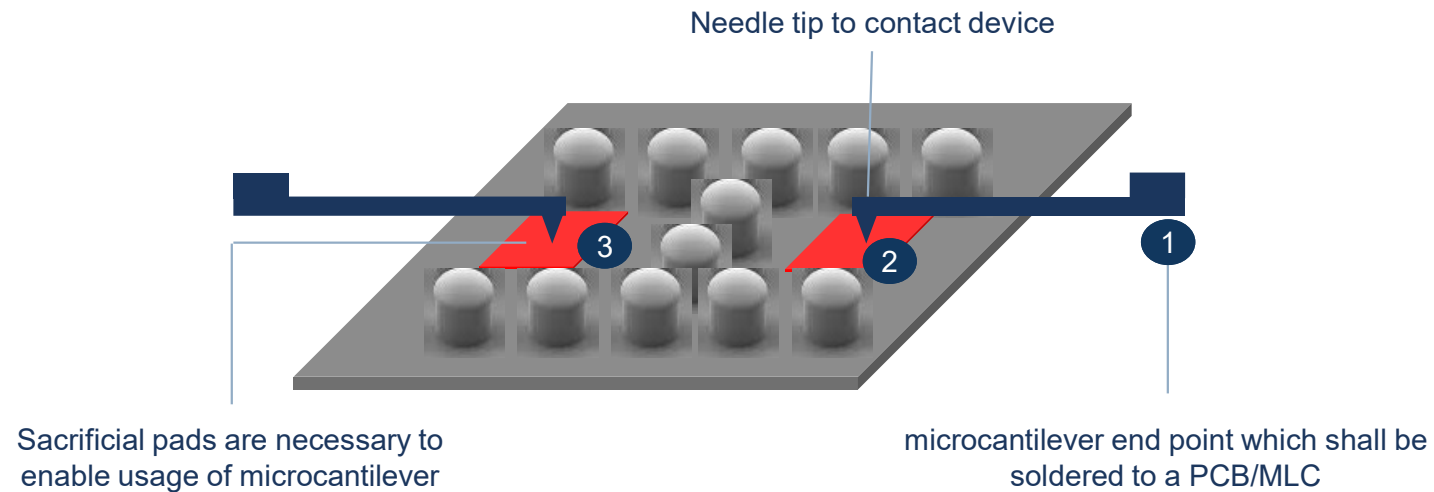
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# HBM Test Flow: microcantilever technology

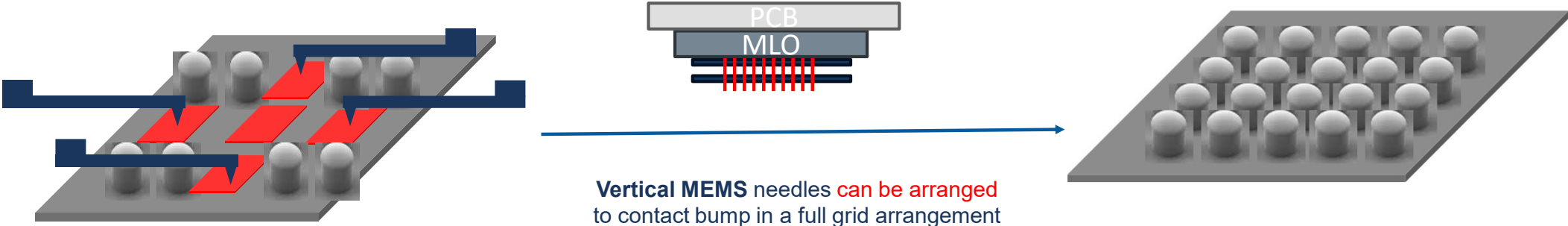
## Microcantilever

needles **cannot be** arranged to contact bump in a full grid arrangement





# HBM Test Flow: vertical mems vs. microcantilever



FRONT END Enter the High Bandwidth Memory (HBM) segment



# FusionLink

## FUSIONLINK

Innovate • Optimize • Accelerate

FusionLink is an advanced interface architecture that combines the best manufacturing technologies & processes to redefine what's possible for test strategy

- FusionLink unifies the know-how across probe cards and device interface boards under one architectural framework
- FusionLink brings together the latest advances in semiconductor packaging and high-performance materials with Technoprobe's proprietary innovations in design, fabrication, assembly, and verification
- The architecture is not a "one size fits all" but is meant to be optimized per project



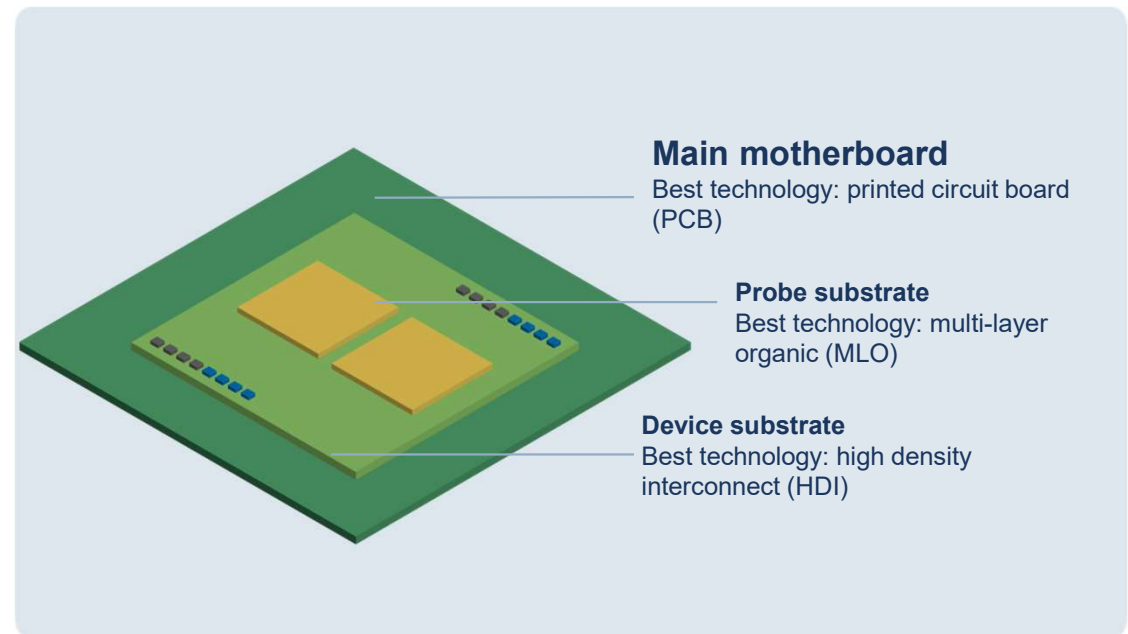
**The Best Performance**



**The Highest Quality**



**Faster Time to Market**





# Financial Outlook



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# Mid-terms scenario\*

## 1 Technological complexity evolution

- Testing solution for Advanced Packaging
- Increase in demand for high-precision tests

## 2 Market trends

- AI will lead the growth for many market segments
- Expansion of memory semiconductor segments

## 3 Geo-political instability

- Technological sovereignty
- Commercial policies

\* As presented during CmD on April 14, 2025



# FY 2025 revenues

Revenues at **628.4€m**

*up 15.7% YoY*



Consistent growth in AI

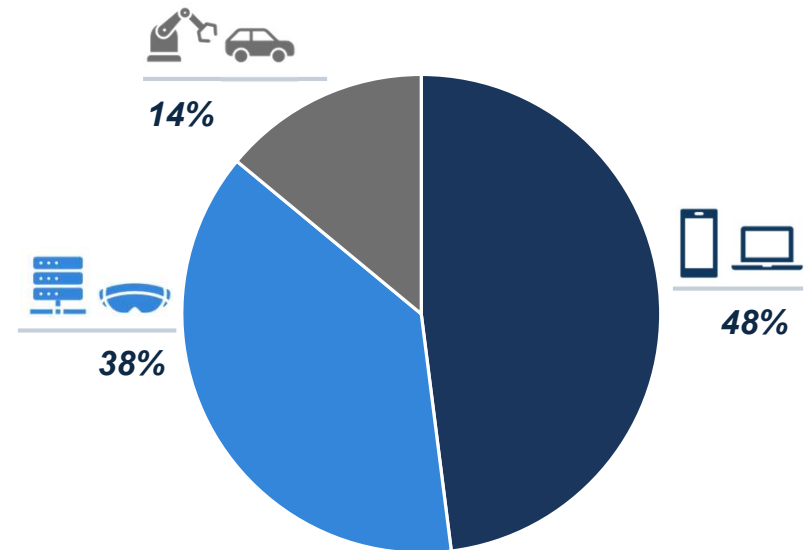


Stabilization of volumes in Consumer market



Softness in Automotive and Industrial

## Split by end markets





# 2026 market outlook & testing perspective

## Geo-Politic Framework

- **Wartime scenario in the Middle East affect worldwide economic stability**
- **Export controls shaping products roadmaps**
- **Supply chain regionalization to offset manufacturing concentration risk**

## Market Drivers: Volumes & Test Intensity

**Structural growth in:**

- **artificial intelligence,**
- **high-performance computing (HPC) and**
- **advanced memory (advanced packaging)**

### Volumes

**Increasing test demand**

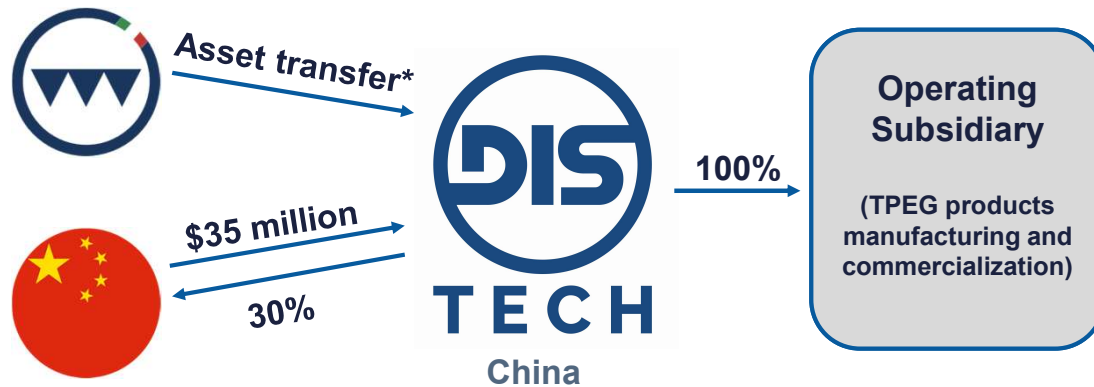
### Technology

**Increasing device architecture complexity which requires more “Known good die” focus**

### Test Intensity

**Higher test intensity across the manufacturing flow**

# 2026 - Agreement in principle to strengthen Chinese market



\*TPEG patents, Equipment, Know-how

## RATIONALE OF THE AGREEMENT

- ✓ Enhance Technoprobe presence in Mainland China through the development of **TPEG technology**
- ✓ Strengthen the **protection of the Technoprobe Group's know-how and Intellectual Property** in the Chinese market
- ✓ Further expand **customer base**
- ✓ Operations expected to gradually ramp end of 2026 / beginning of 2027

## TERMS OF AGREEMENT

- Investment from a Chinese partner of \$35m expected to be implemented through the **subscription of a reserved capital increase to be resolved by DIS China** following which the new partner would hold an equity interest of approximately 30% in DIS China; the execution will in any event **be subject to the obtaining of authorization from the competent Italian authority under Golden Power regulations**, as well as the completion of the required approval process before the relevant Chinese authorities (including the State Administration of Foreign Exchange and the State Administration for Market Regulation), and to certain other customary conditions precedent.
- Incorporation by DIS China of **an operating subsidiary** in the Suzhou area, which will be entrusted with the **manufacturing and distribution** of TPEG-based products
- Agreement, reached in its essential terms, **will be formalized by the end of March** through the execution of the relevant definitive agreements.



# Q1 2026 market drivers



Strong growth in AI



Slight growth in Consumer market



Recovery in Automotive and Industrial

**Revenues at 187.0 €m**

*up 15.6% QoQ*

*up 19.0% YoY*

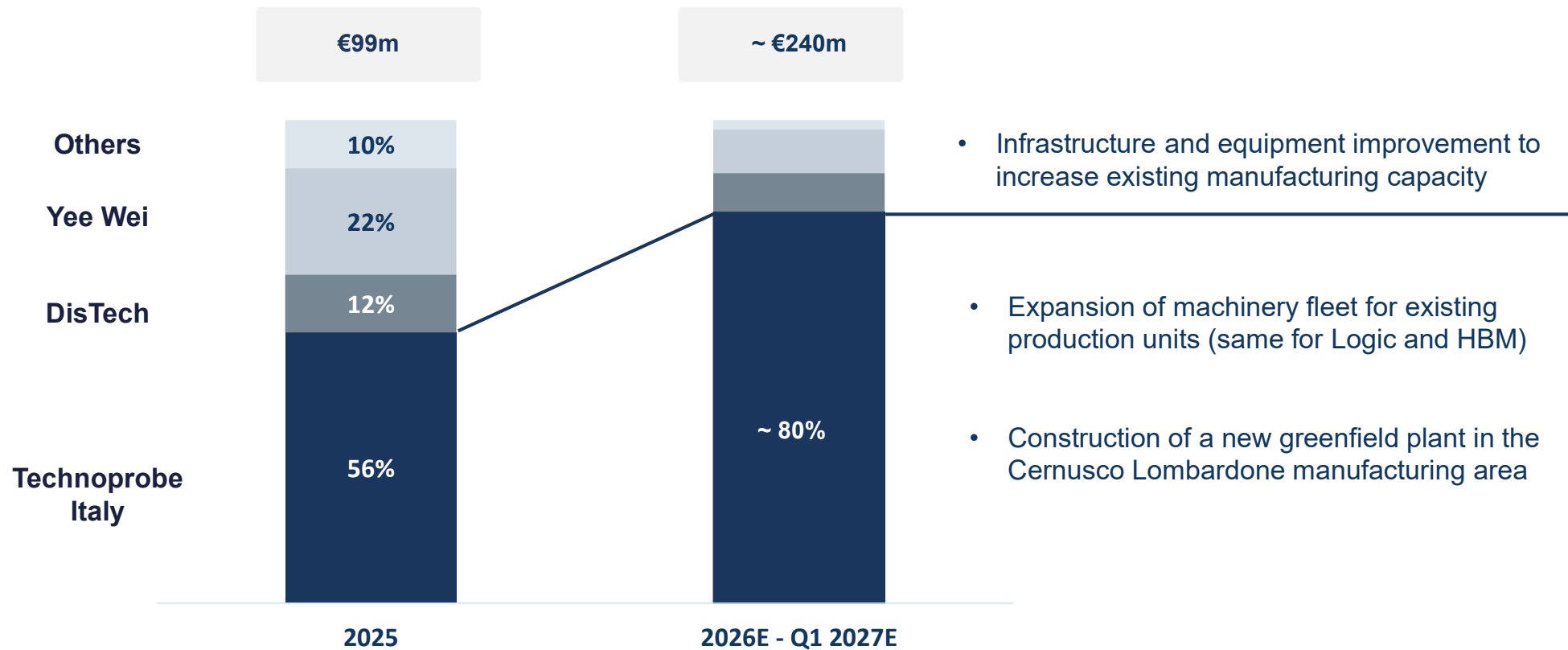


# Q1 2026 results

	Q1 2026	Q1 2025	YoY%	Notes
<b>Revenues (€m)</b>	187.0	157.2	<b>+19.0%</b>	<ul style="list-style-type: none"> <li>• <b>Organic growth:</b> strong contribution from AI, slight growth in Consumer and recovery in Automotive and Industrial</li> <li>• <b>FX negative impact</b> of €20m</li> </ul>
<b>Gross Profit (€m)</b>	91.1	70.8	<b>+28.7%</b>	<ul style="list-style-type: none"> <li>• Increasing <b>manufacturing capacity</b></li> <li>• Ongoing recovery in <b>production efficiency</b></li> <li>• <b>Operating leverage</b></li> </ul>
<i>% margin</i>	48.7%	45.0%	<b>+370 bps</b>	
<b>Ebitda (€m)</b>	69.2	48.0	<b>+44.2%</b>	<ul style="list-style-type: none"> <li>• <b>Ebitda margin</b> benefited from the aforementioned operating leverage with stable R&amp;D or SG&amp;A</li> </ul>
<i>% margin</i>	37.0%	30.5%	<b>+650 bps</b>	
<b>Net Financial Position (€m)</b>	Mar 31, 2026 660.5	Dec 31, 2025 684.2	<b>Variance mainly</b> attributable to <b>cash flow from operating</b> activities (+2€m), and the <b>unrealized FX impact</b> on foreign currency bank accounts (+8€m), more than offset by <b>Capex</b> of the period (-34€m)	





# Capex to Support Organic Growth



# Cernusco Lombardone (Italy) - plant expansion 26-27



**+4,000 sqm manufacturing area ready end of Q1 2027**

-  Current footprint
-  Greenfield under construction



# Q2 2026 Guidance

**Revenues: €266m**

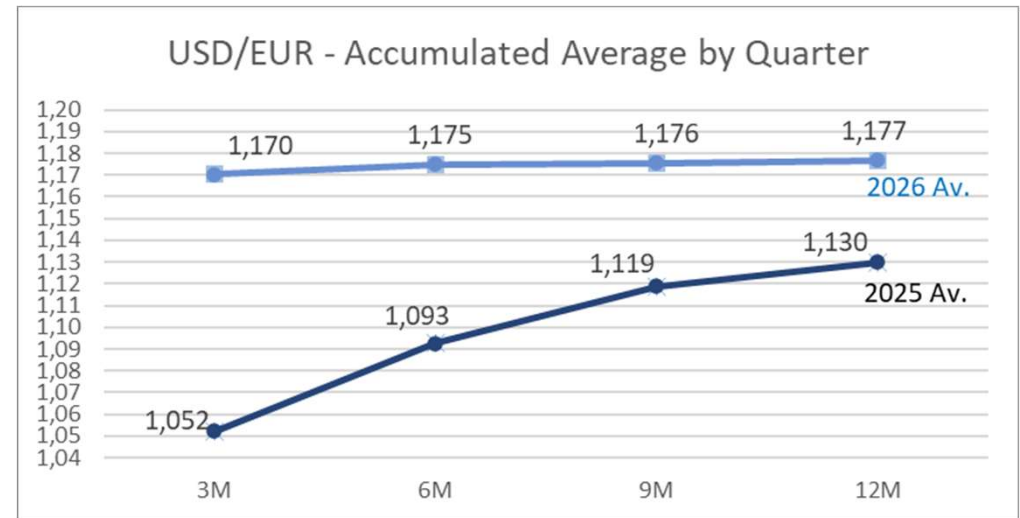
(+/-3%)

**Gross Margin: 55%**

(+/-200bps)

**Ebitda Margin: 45%**

(+/-200 bps)



Average	Q1 '25	Q2 '25	Q3 '25	Q4 '25
3M	1,052	1,134	1,168	1,163
6M	1,052	1,093		
9M		1,119		
12M			1,130	

Average	Q1 '26	Q2 '26*	Q3 '26*	Q4 '26*
3M	1,170	1,180	1,177	1,180
6M	1,170	1,175		
9M		1,176		
12M			1,177	

\*Estimate



# 2027 targets anticipated with new 2026 targets

