



Technoprobe S.p.A. Company Presentation

March, 2026



Disclaimer

This document has been prepared by Technoprobe S.p.A. (the “Company”) solely for use in the presentation.

This document does not constitute or form part of any offer or invitation to sell, or any solicitation to purchase any security issued by the Company. The information contained and the opinions expressed in this document have not been independently verified. In particular, this document may contain forward-looking statements that are based on current estimates and assumptions made by the management of the Company to the best of its knowledge. Such forward-looking statements are subject to risks and uncertainties, the non-occurrence or occurrence of which could cause the actual results– including the financial condition and profitability of the Company – to differ materially from or be more negative than those expressed or implied by such forward-looking statements. This also applies to the forward-looking estimates and forecasts derived from third-party studies.

Consequently, neither the Company nor its management can give any assurance regarding the future accuracy of the estimates of future performance set forth in this document or the actual occurrence of the predicted developments. The data and information contained in this document are subject to variations and integrations.

Although the Company reserves the right to make such variations and integrations when it deems necessary or appropriate, the Company assumes no affirmative disclosure obligation to make such variations and integrations.



Innovation begins with us

A leading company in the field of semiconductors and microelectronics



INNOVATION BEGINS WITH US

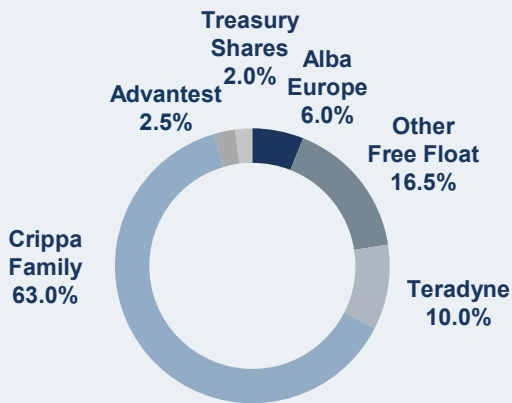
Company Overview



2025 Key financial metrics

Revenue	Ebitda	Net Income	Net Financial Position	Mkt Cap
€628.4m +16% YoY	€201.4m 32% EBITDA margin	€98.8m 16% on revenues	€684.2m as at 12/31/2025	~€8,7bn as at 3/20/2026

Shareholding Structure

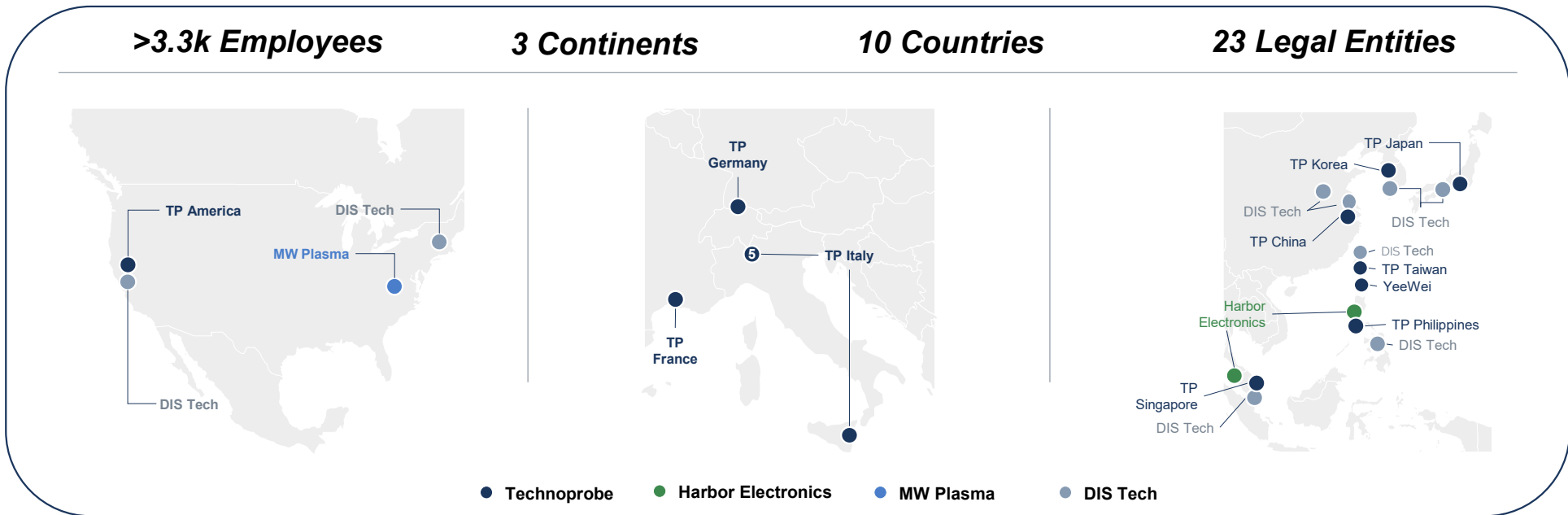


- 
 Leading player in designing and manufacturing of **probe cards to test Logic chips**
- 
 Manufacturing process **vertical integrated**
- 
 Strong focus on **innovation**
- 
 Extensive **global presence** and widespread **local footprint**



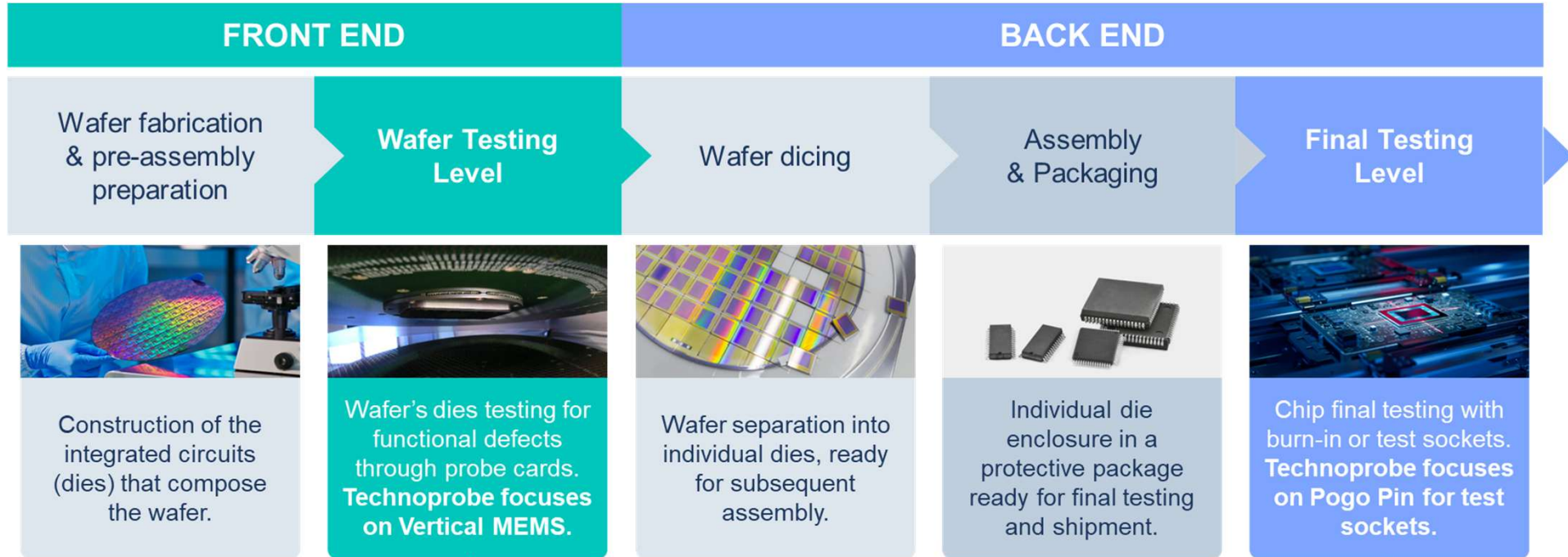
Where we are

Headquartered in Italy with branches in Europe, America, and Asia



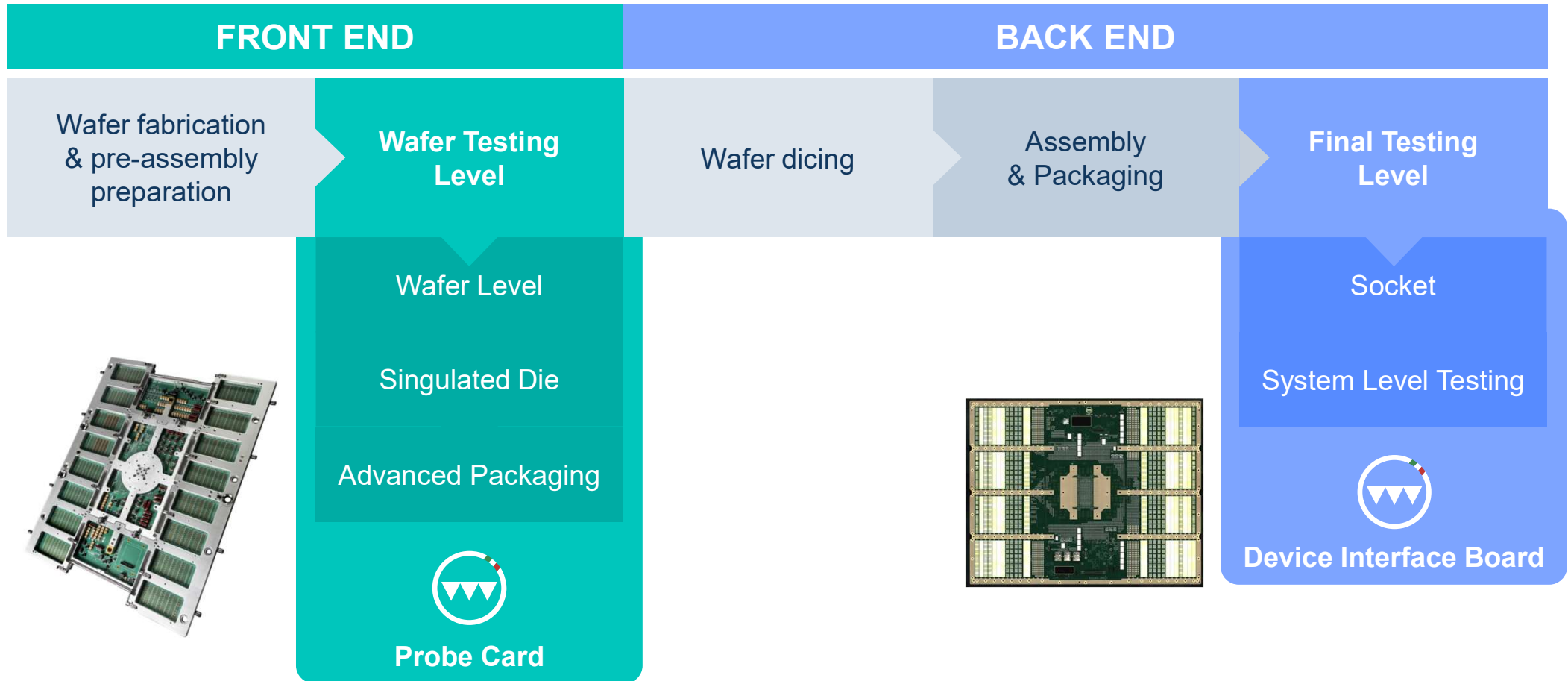


Testing in the semiconductor manufacturing process



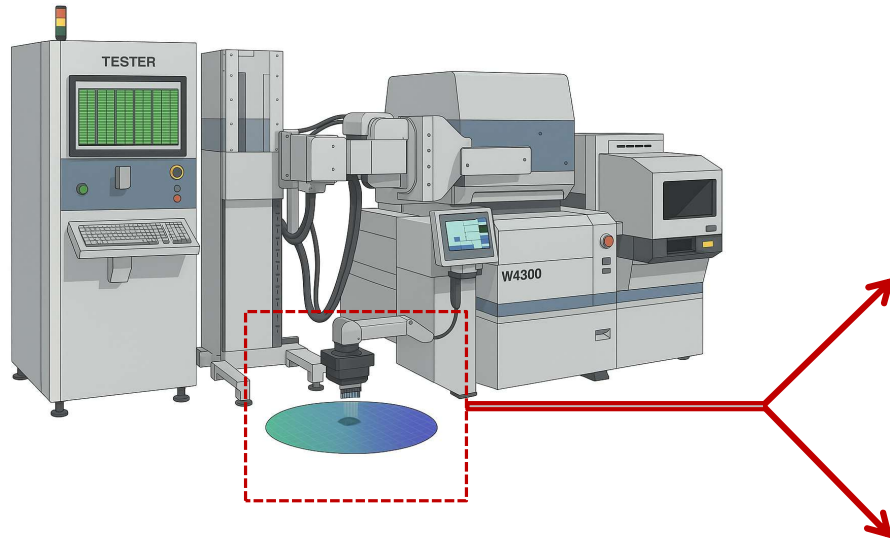


Our positioning in the testing space





The testing phase



Tester (ATE)

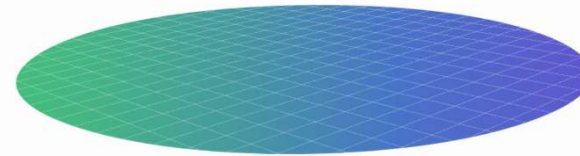
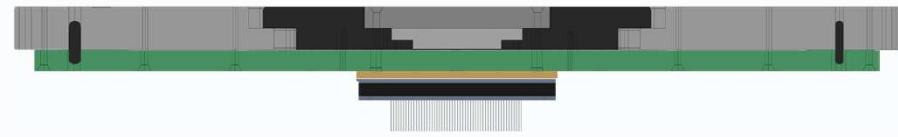
- A tester, or Automated Test Equipment (ATE), applies electrical signals to semiconductor devices and measures their responses to verify performance and functionality
- ATE systems execute test programs to identify manufacturing defects and ensure chips meet design specifications



Probe Card



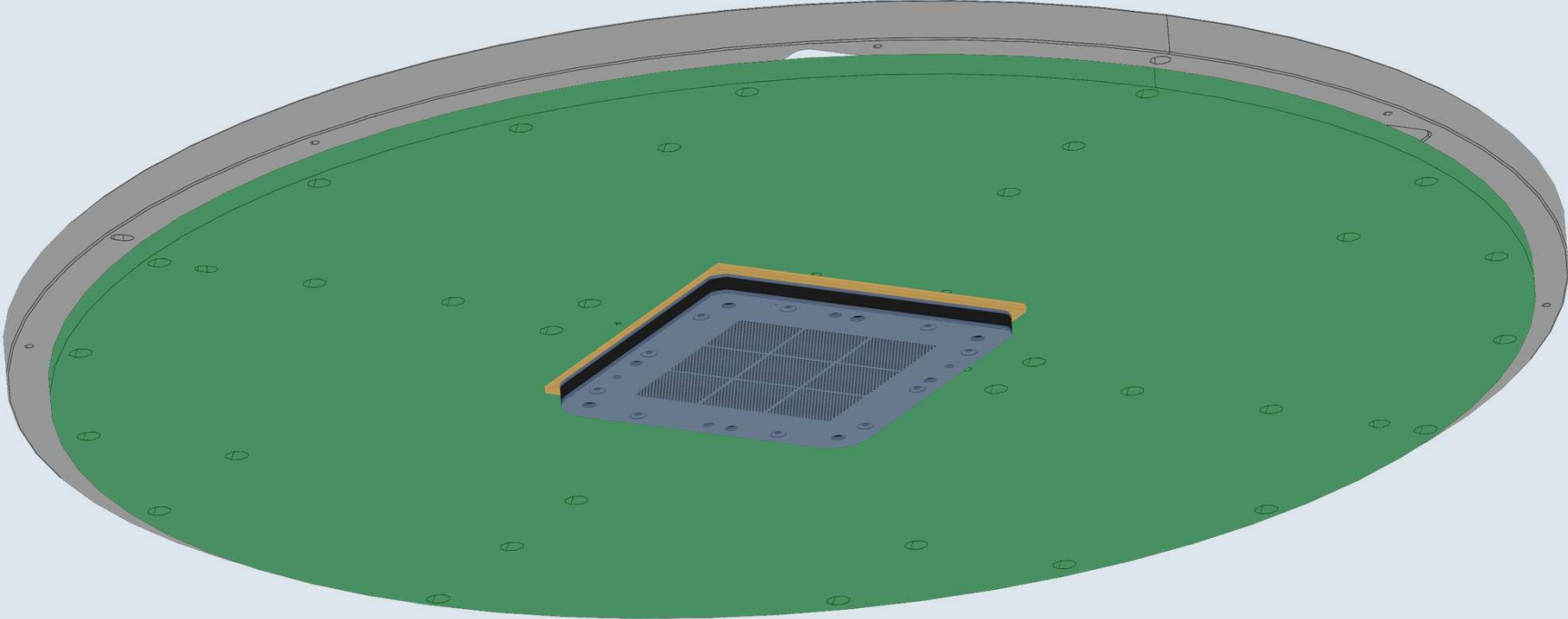
- A probe card is a precision device with microscopic needles or MEMS tips that make electrical contact with each die's test pads on the wafer
- The probe card interconnect a tester (ATE) with dies on a wafer or diced dies for electrical testing.



Wafer

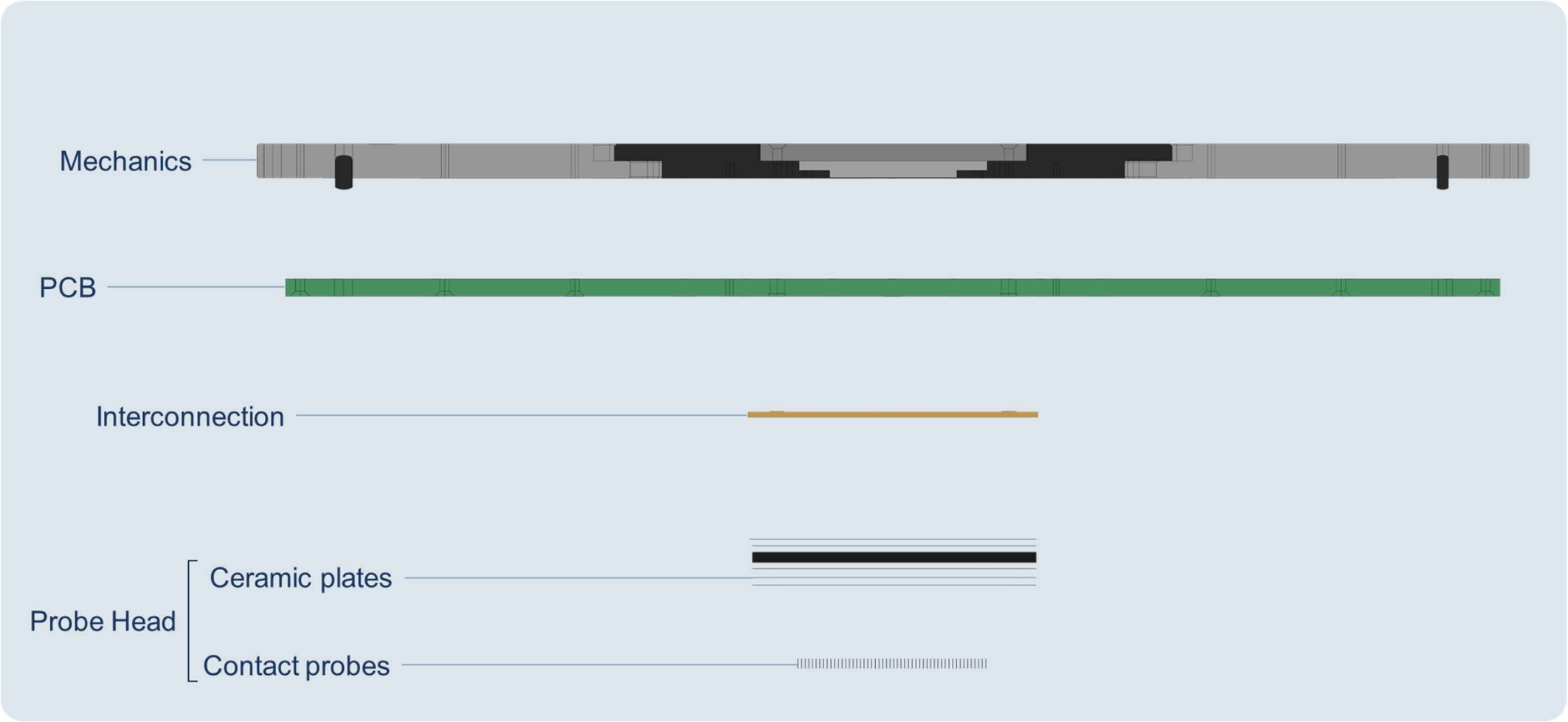
- A wafer is a thin, circular semiconductor substrate (most commonly silicon) on which integrated circuits (dies) are fabricated
- Each die functions as an individual integrated circuit that, once separated (diced) and packaged with external connectors, becomes a finished semiconductor chip

The Probe Card





The Probe Card





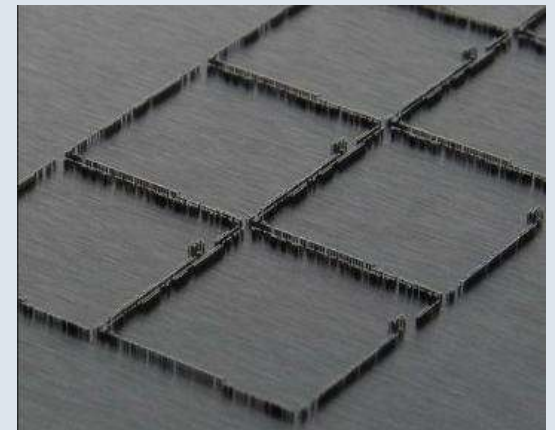
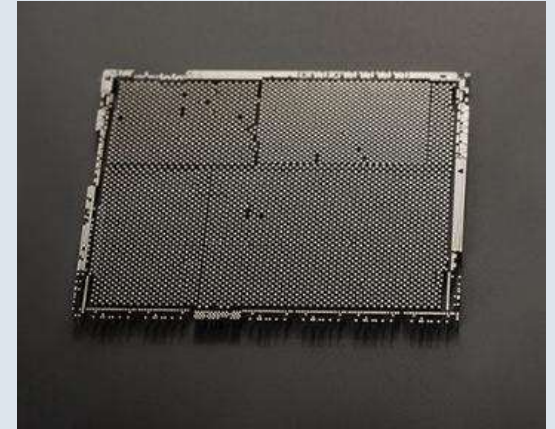
The Probe Card

Facts Sheet

1 probe card

100000+	Number of contacts interconnecting tester with device
1000A+	Ampere of currents to supply the device
20 μ m	Pad pitch to ATE space transformation of a factor >10x
100W+	Watts of power to dissipate through the card
200Kg+	Withstand a force of hundred kilograms
-60°C / +175°C	Wide supported operation temperature range

All requirements satisfied within a 10cm x 10cm x 1cm 3D space





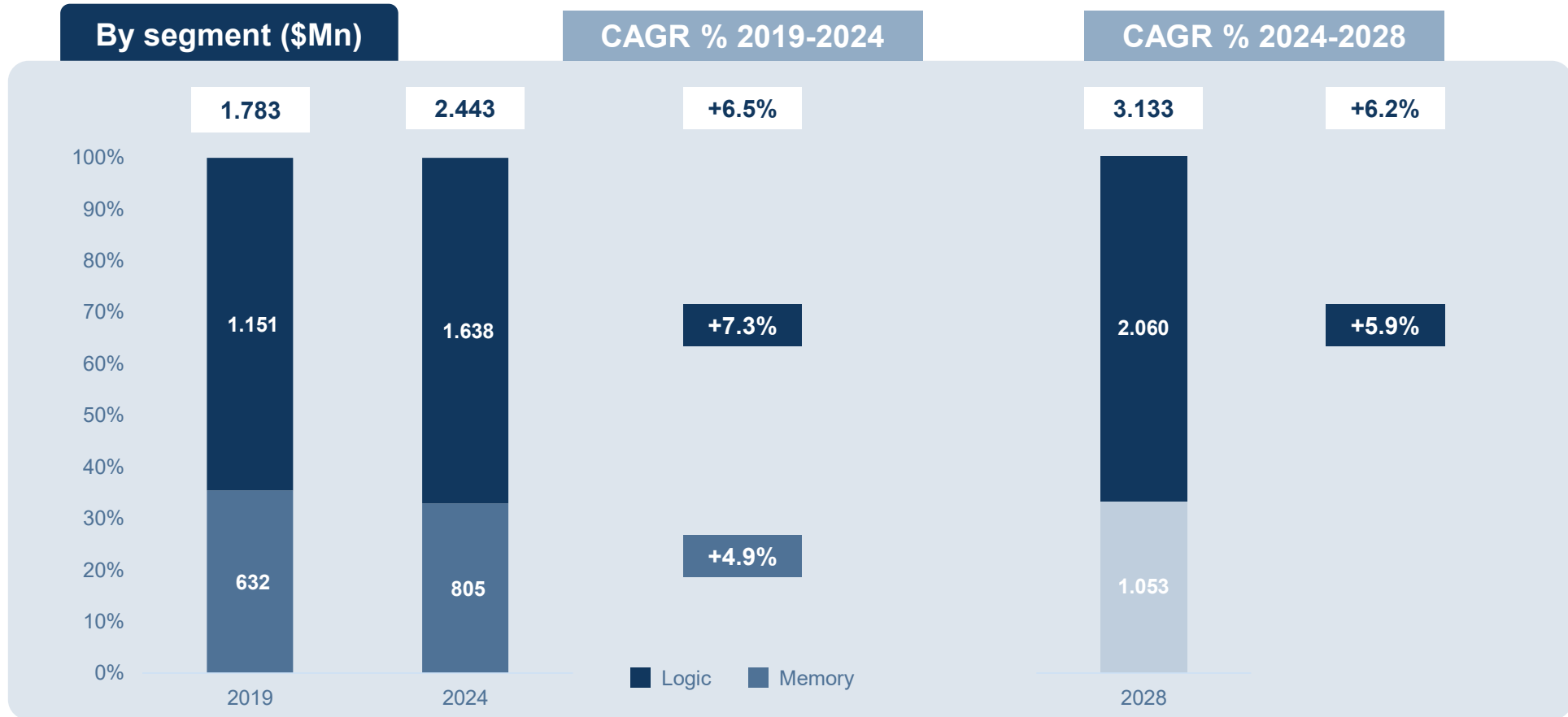
Reference Market



INNOVATION BEGINS WITH US



Overview of the Semiconductor Probe Cards market

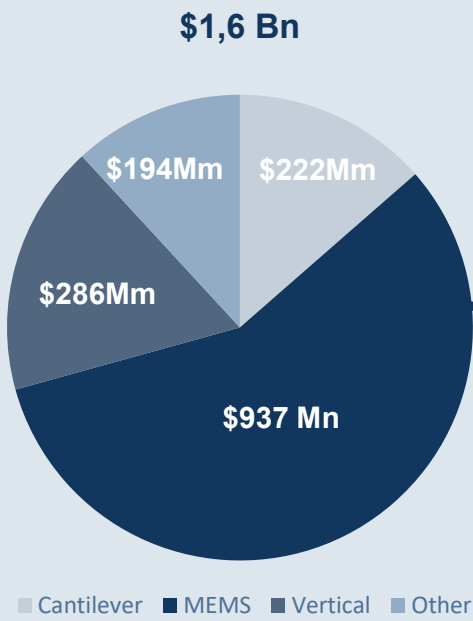


Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept. 2024) – rounded figures. Memory: DRAM+NVM & Other memory. Logic: MEMS, Power, RF, CMOS Image Sensors, Photonics, Other non-memory, WAT.



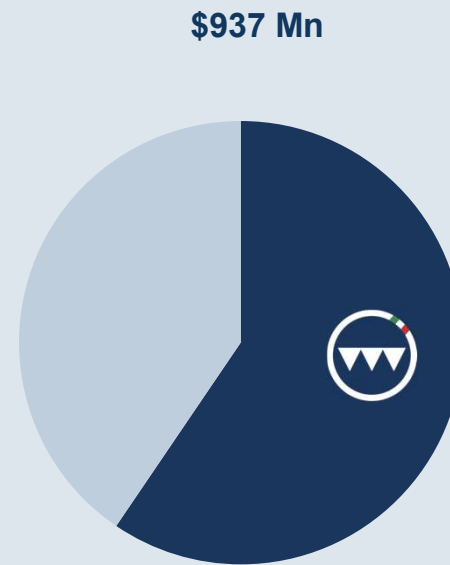
Our reference market

2024 Logic Probe Card market



Market Share: 34%

2024 MEMS Logic Probe Card

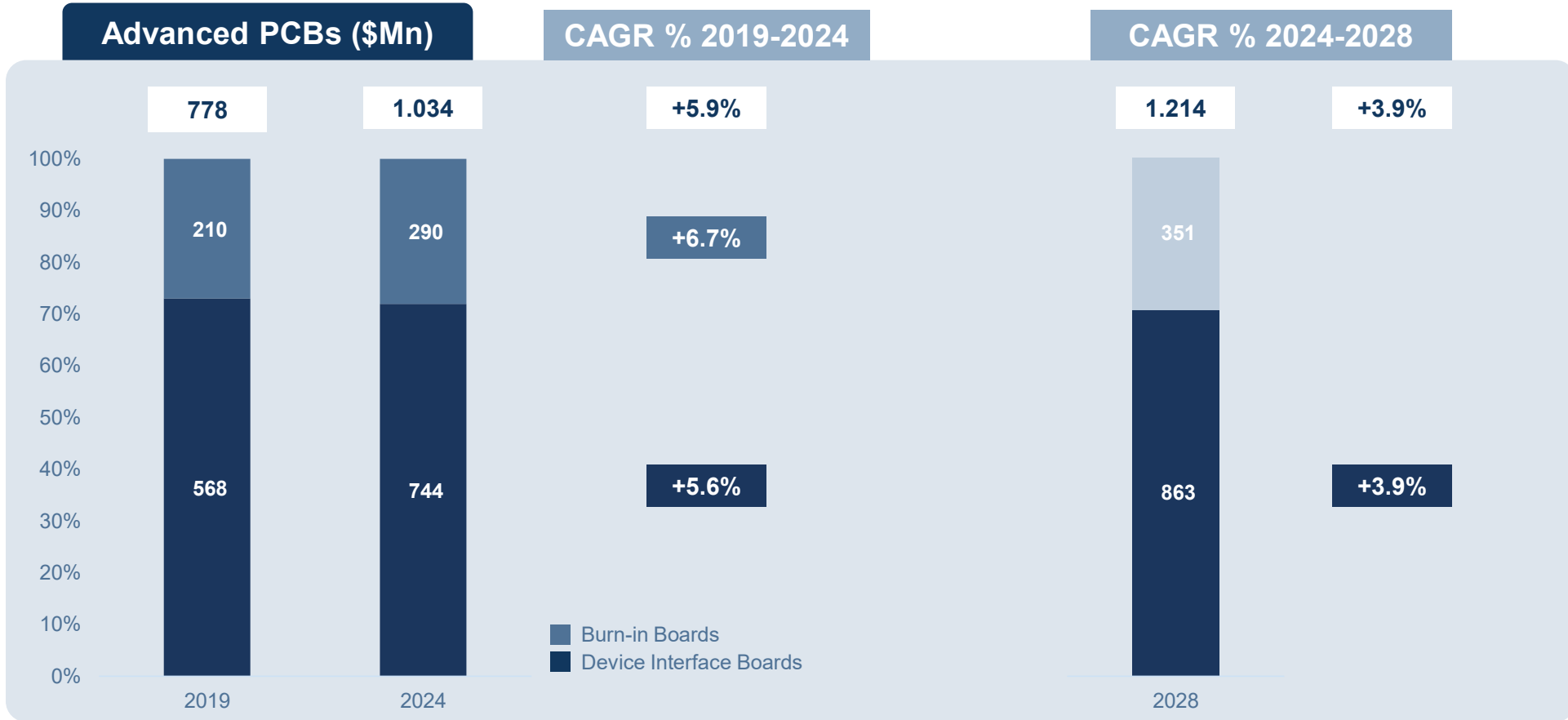


Market Share: 60%

Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.



Final Testing market – Advanced PCBs



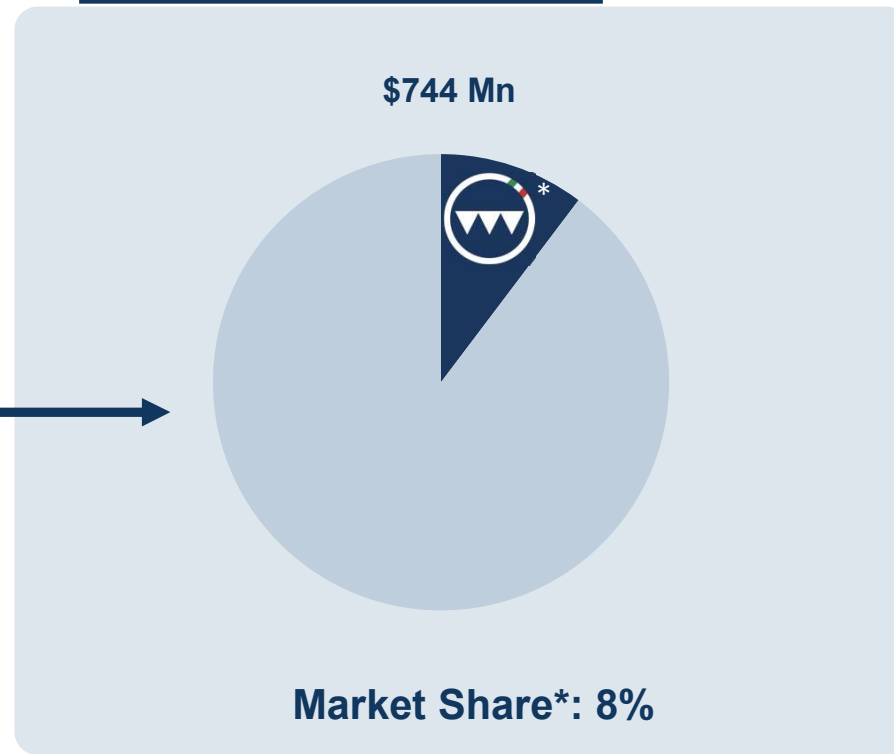
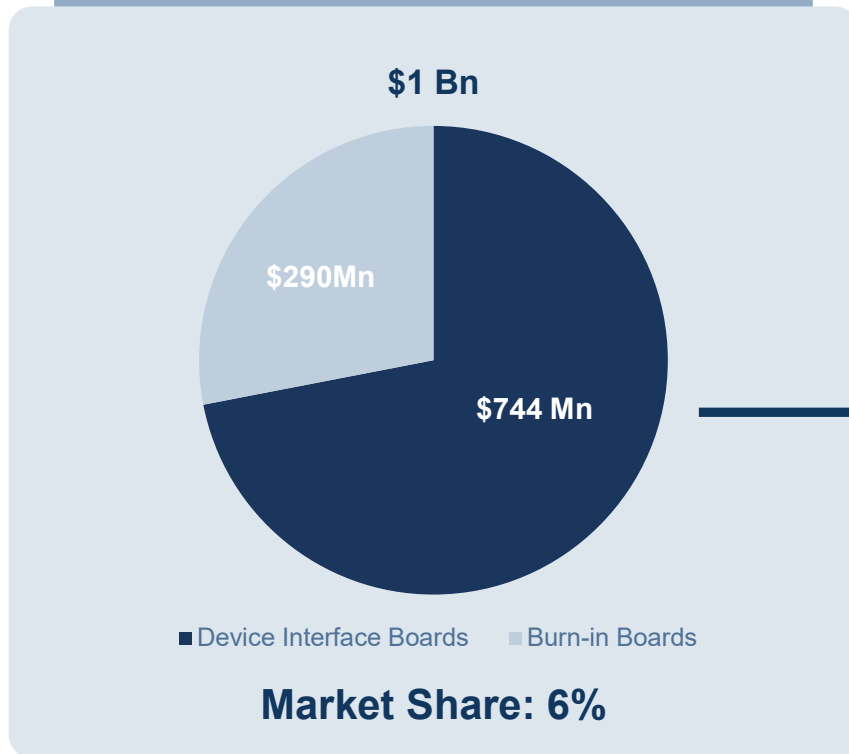
Source: Yole Test Interface Board market monitor Q3 2024 (Sept. 2024) – rounded figures.



Final Testing market – Our reference market

2024 Advanced PCB for semiconductor

2024 Final Test DIB market



Source: Yole Test Interface Board market monitor Q3 2024 (Sept. 2024) – rounded figures.
(*) Based on DIS Tech Final Test FY24 data. Company acquired by Technoprobe on May 27, 2024.



Business Model



INNOVATION BEGINS WITH US



A successful and vertically integrated business model



Supported by an open eco-system partnerships



TERADYNE

Accelerate growth of
complete Probe Card and
Final Test Interfaces by
acquisition of DIS

Joint Development Projects
to deliver superior customer
value in SOC and Memory



TECHNOPROBE

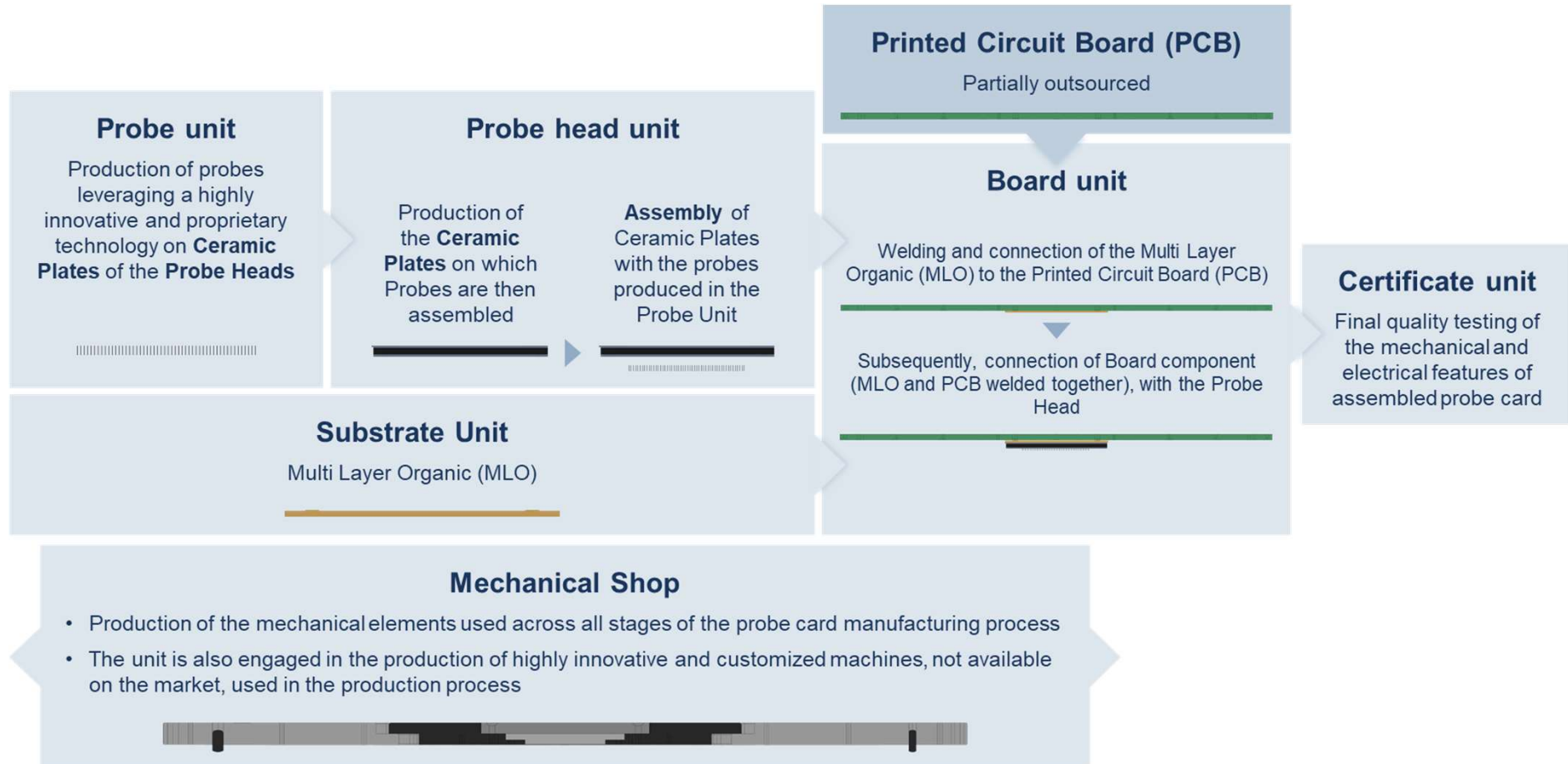
ADVANTEST

Priority suppliers
of PCB

Joint Development Projects
to share knowledge



The Probe Card manufacturing process

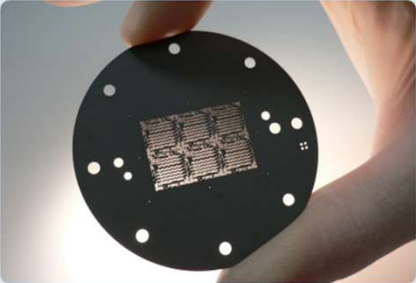




A wide range of highly innovative technologies inside

Advanced micromachining

Advanced laser cutting:
high accuracy and fast lead time



Thin film

Strong investment in advanced thin film technology to reduce lead time and improve quality and complexity



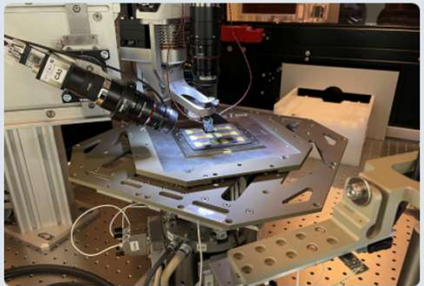
3D MEMS

Acquisition of MICROFABRICA in 2019; the sole company in the world specialized in 3D metallic MEMS manufacturing



Advanced manufacturing

Advanced manufacturing for high volume and best quality assembly of micro components





Vision & Strategy



INNOVATION BEGINS WITH US



Challenges & strategic setting

1 Evolution of chip technology (more than Moore)

Scaling slow down as enabler for **chiplets**,
3D architectures and **new materials**

→ **Continuous investments in R&D**

→ **M&A as accelerator of
technological development**

2 Increase in complexity

Design and manufacturing are becoming essential
capabilities to reliably deliver **complex solutions**

→ **Strategic partnerships**

→ **Vertical integration of the most value-
added components of the probe card**

3 Client satisfaction

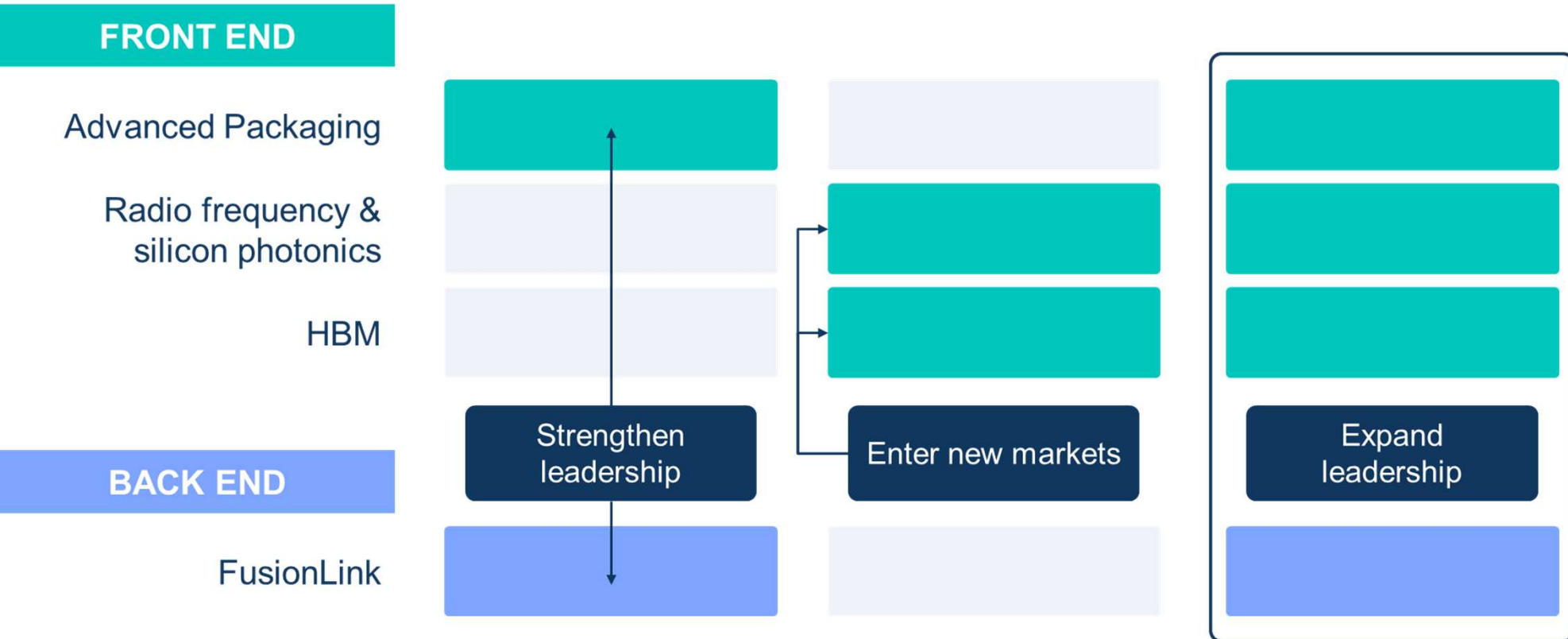
Reliability of the product & on-time delivery

→ **Support on site**

→ **Commercial agreements**

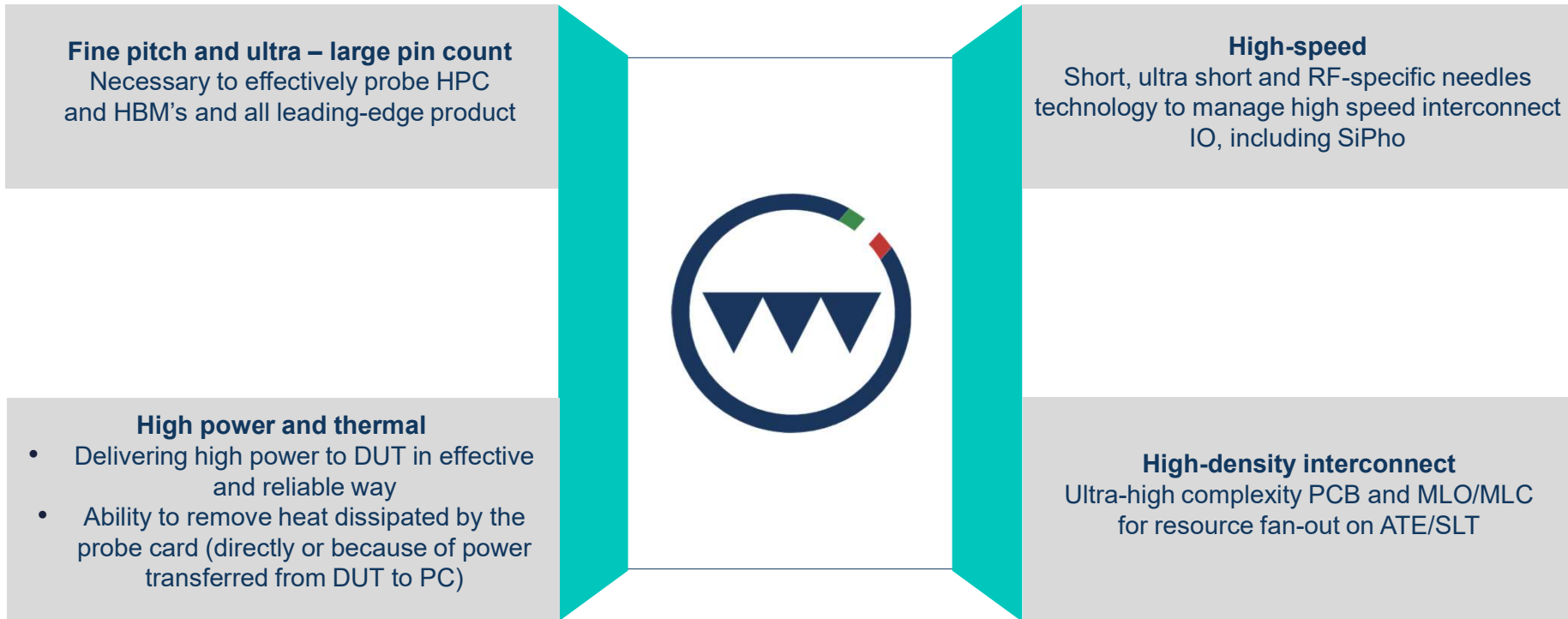


Growth drivers & trajectories





Technoprobe as advanced packaging enabler





A hungry world of wideband applications



Exponential increase in number & type of connected things



Increasing reliance on the cloud



Bandwidth-hungry applications

Analog radio frequency

Satellite communications and sensing, automotive radar, mobile communication,...



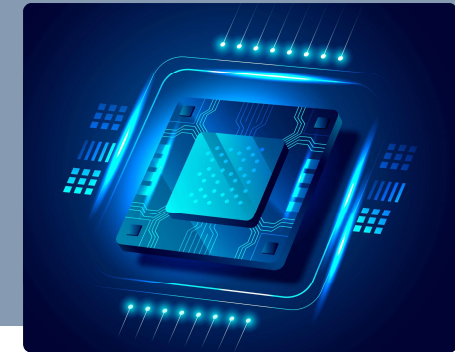
Chiplet probing

High density and high-speed IO inside chiplet demand for high-performance probe needles



Silicon photonics

Chiplet to chiplet interconnect / photonics-driven computing

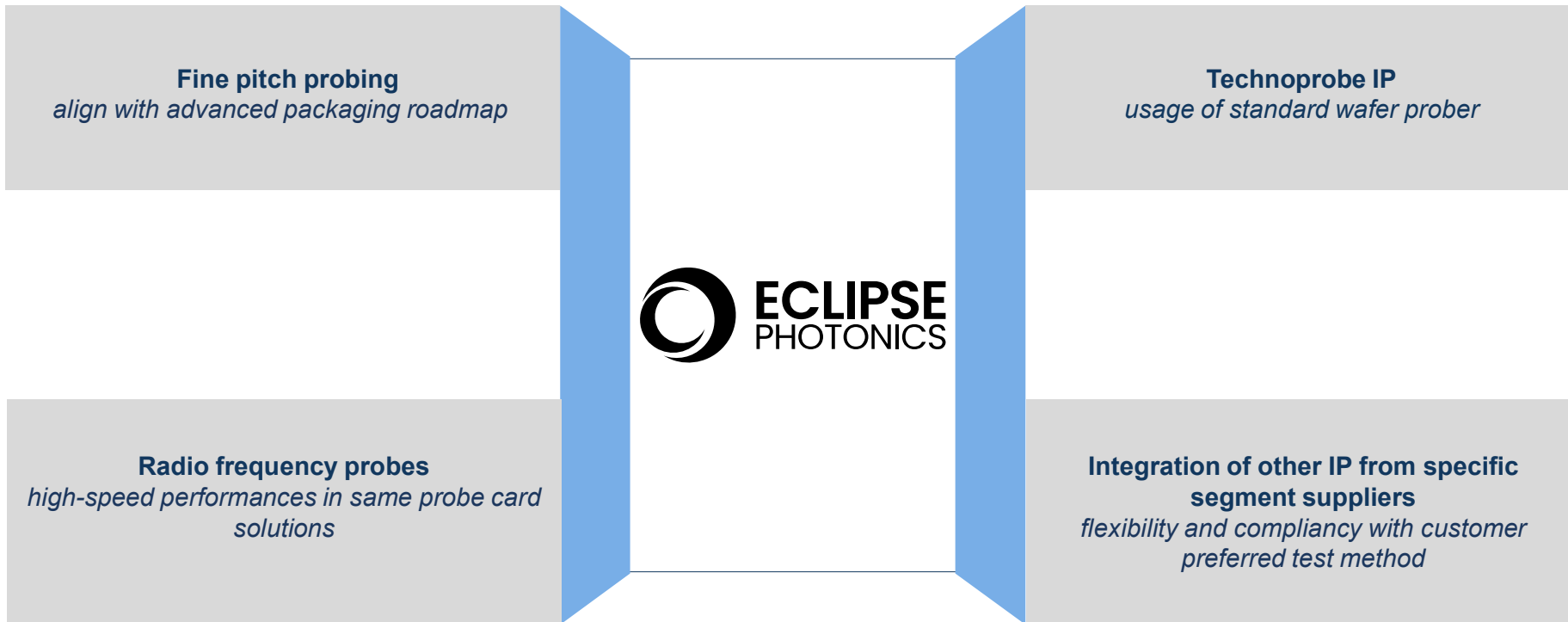


FRONT END Proliferate radio frequency and silicon photonics

INNOVATION BEGINS WITH US



Technoprobe silicon photonics testing solution



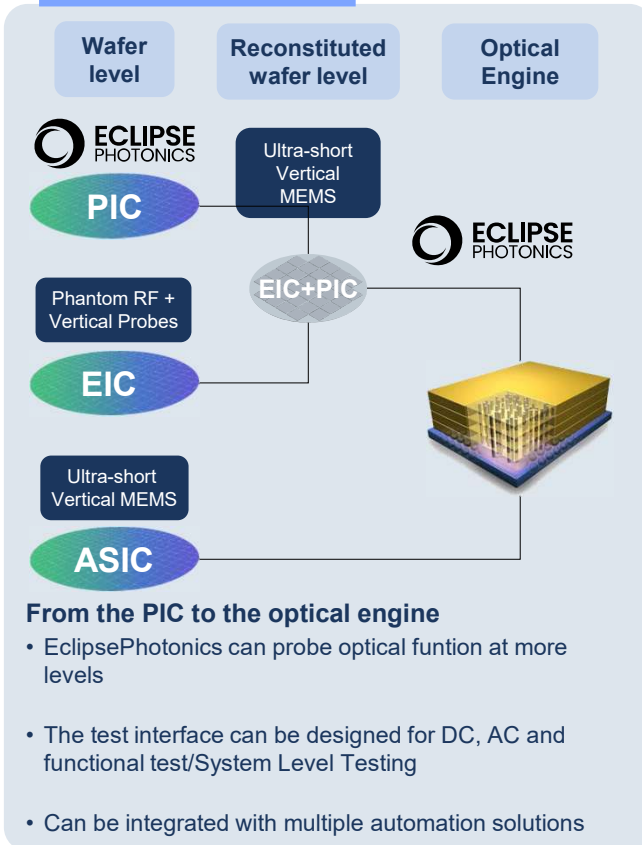
FRONT END Proliferate radio frequency and silicon photonics

INNOVATION BEGINS WITH US



Eclipse photonics

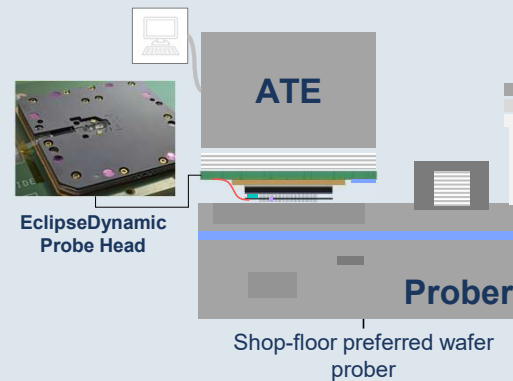
Where it applies



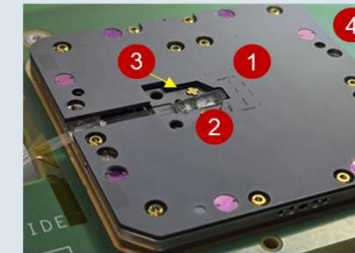
How it works

An autonomous instrument

- EclipsePhotonics embeds the electronics to autonomously operate when on the tester
- It integrate a programmable unit to execute the alignment algorithm(s), interface to the tester and operate the electronics
- The integration with ATE gives the capability to control the instrument from the user test program



What it delivers



Probe card content

1. Vertical MEMS needle and Phantom RF probes
2. FAU, fiber optics and optical connector (blind mated)
3. FAU positioner (up to 6-axis)
4. Electronics to activate and control the positioner

What it delivers

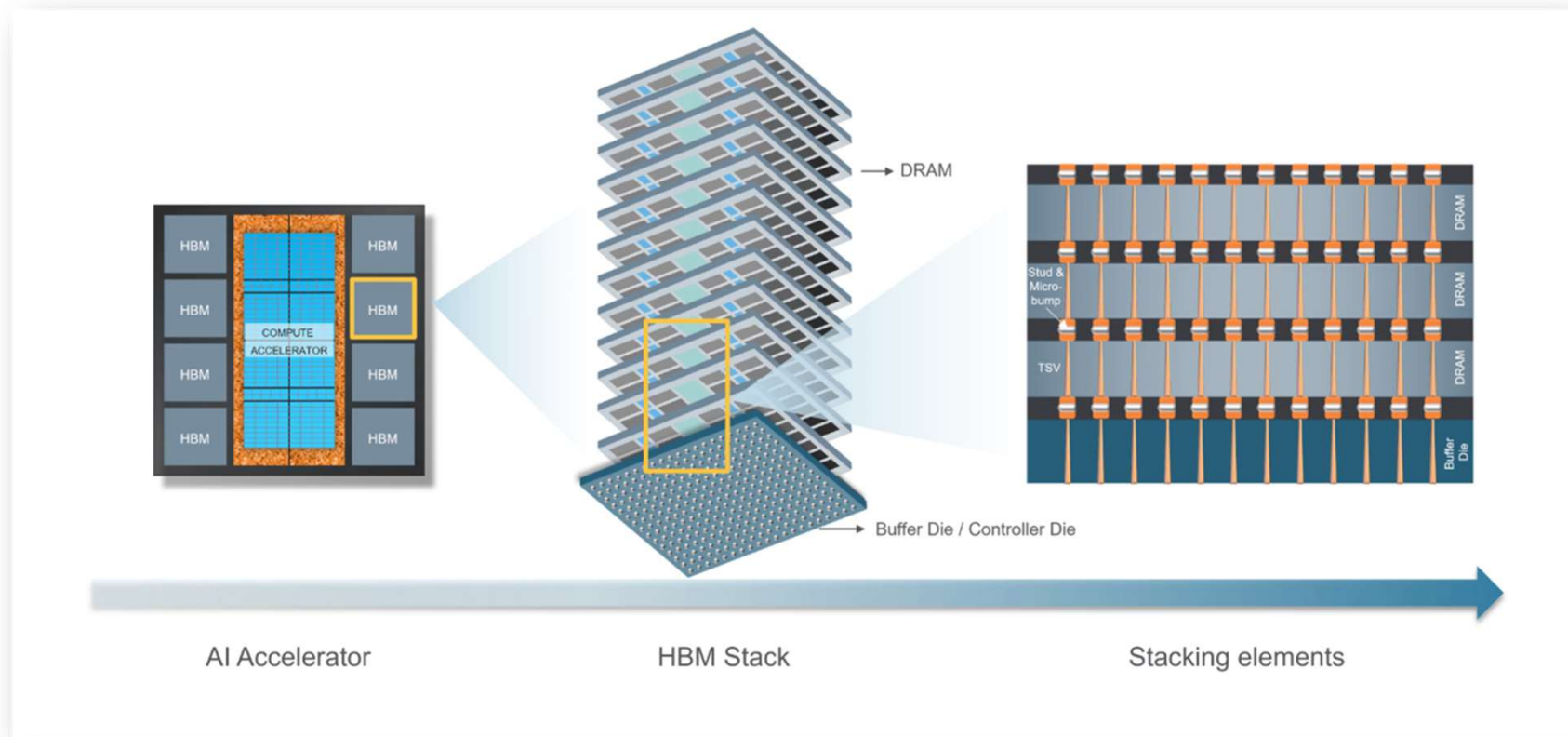
- Direct docking
- Integrated optical and electrical probe, with off-line card certification
- High operation stability, repeatability and immunity to external factors
- In-field repairability
- Minimal optical to electrical pin distance constraints

PIC: photonics integrated circuit **EIC:** electronic integrate circuit **ASIC:** Application-Specific Integrated Circuit

FRONT END Proliferate radio frequency and silicon photonics

INNOVATION BEGINS WITH US

HBM Architecture



Cartoon credit: Applied Material web site

FRONT END Enter the High Bandwidth Memory (HBM) segment

INNOVATION BEGINS WITH US

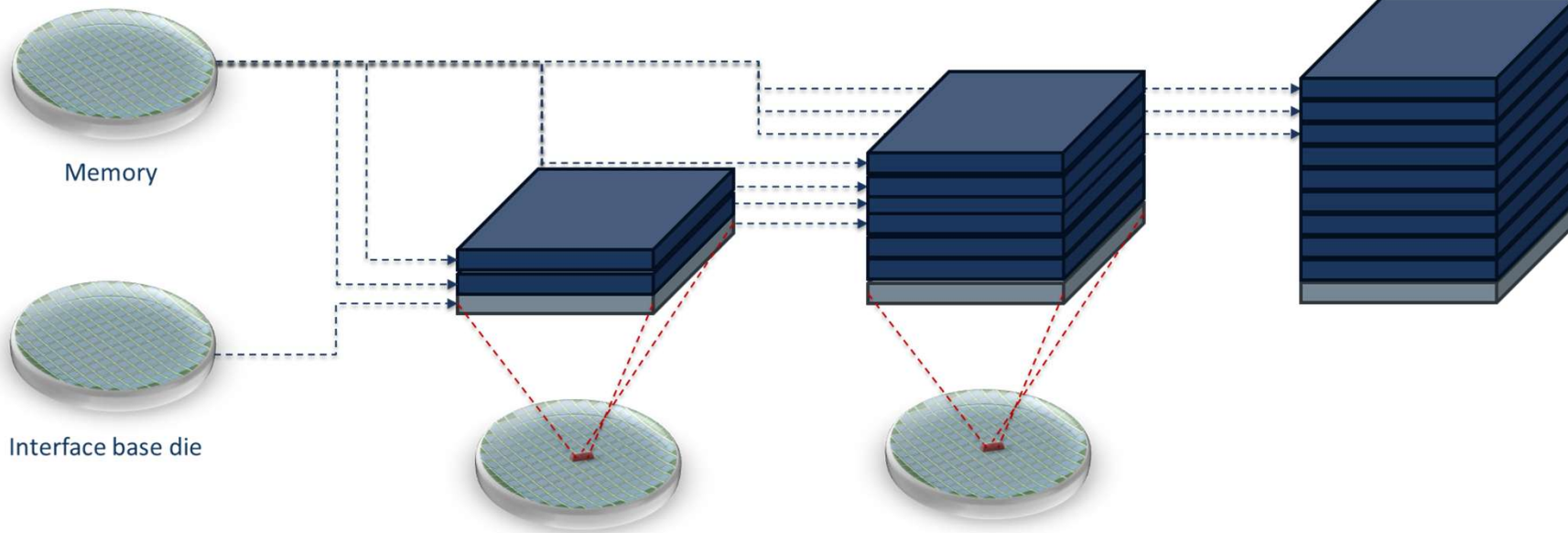


HBM Test Flow

Wafer level

Intermediate ?
Reconstituted wafer level

HBM cube
Singulated Die level



Raw Defects

Interconnect

Interconnect

Performances

Logic
Base die

Memory
Sacrificial

Sacrificial

Sacrificial

FRONT END Enter the High Bandwidth Memory (HBM) segment

INNOVATION BEGINS WITH US

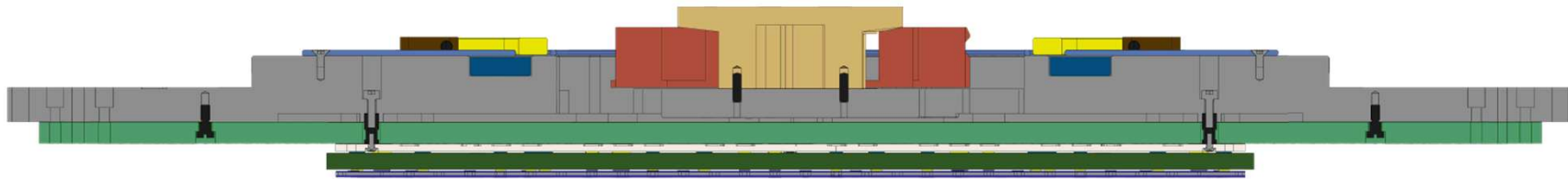


HBM: new testing solution

DRAM and HBM are typically tested with **microcantilever** probing technologies.

Most **advanced HBM** and Next Generation products are becoming more challenging in terms of pad pitch, signal integrity, and power.

For both applications Technoprobe is leveraging on **Vertical MEMS** solution and on a unique PC architecture.



FRONT END Enter the High Bandwidth Memory (HBM) segment

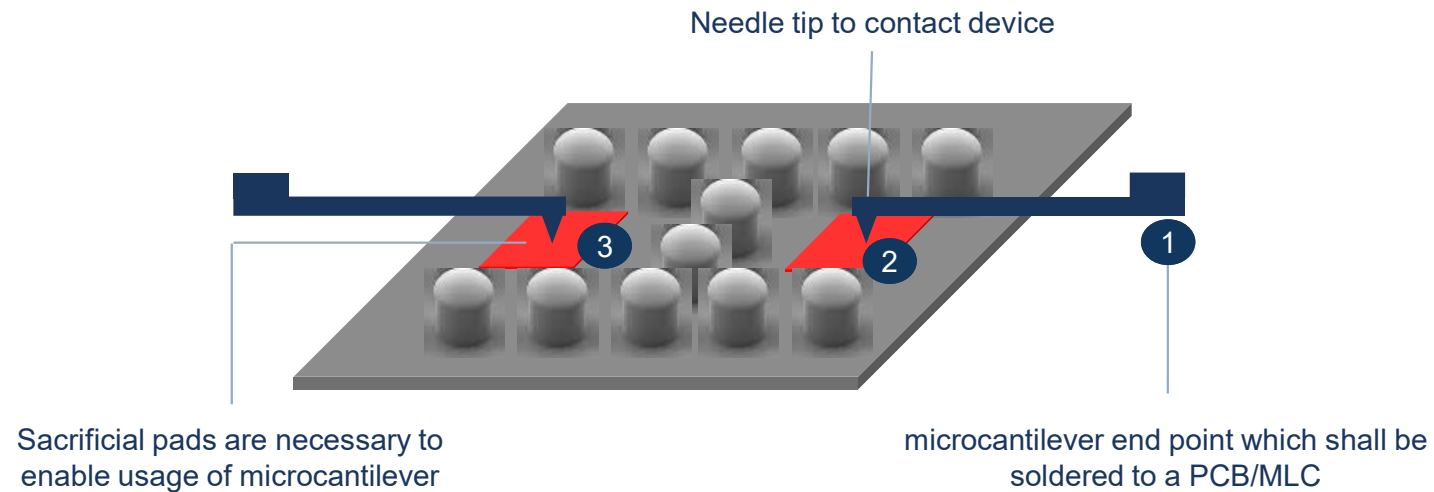
INNOVATION BEGINS WITH US



HBM Test Flow: microcantilever technology

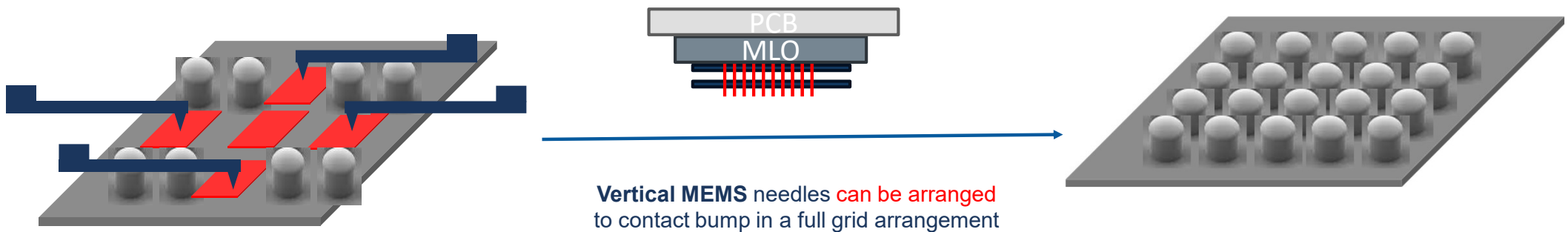
Microcantilever

needles **cannot be** arranged to contact bump in a full grid arrangement





HBM Test Flow: vertical mems vs. microcantilever





FusionLink

FUSIONLINK

Innovate • Optimize • Accelerate

FusionLink is an advanced interface architecture that combines the best manufacturing technologies & processes to redefine what's possible for test strategy

- FusionLink unifies the know-how across probe cards and device interface boards under one architectural framework
- FusionLink brings together the latest advances in semiconductor packaging and high-performance materials with Technoprobe's proprietary innovations in design, fabrication, assembly, and verification
- The architecture is not a "one size fits all" but is meant to be optimized per project



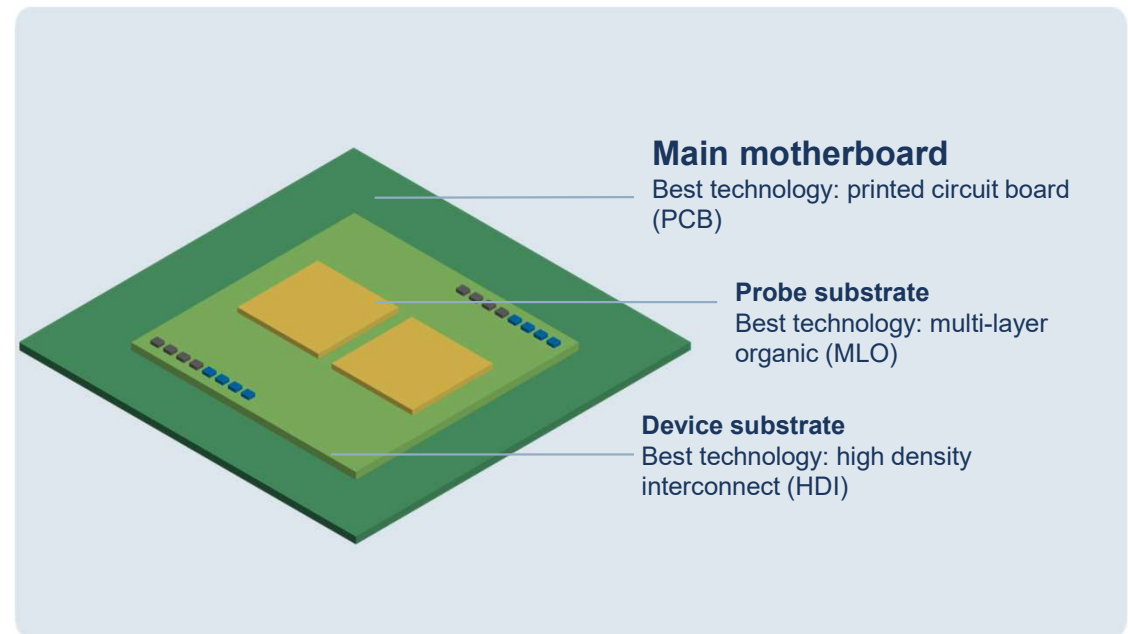
The Best Performance



The Highest Quality



Faster Time to Market





Financial Outlook



INNOVATION BEGINS WITH US



Mid-terms scenario*

1 Technological complexity evolution

- Testing solution for Advanced Packaging
- Increase in demand for high-precision tests

2 Market trends

- AI will lead the growth for many market segments
- Expansion of memory semiconductor segments

3 Geo-political instability

- Technological sovereignty
- Commercial policies

* As presented during CmD on April 14, 2025



FY 2025 revenues

Revenues at **628.4€m**

up 15.7% YoY



Consistent growth in AI

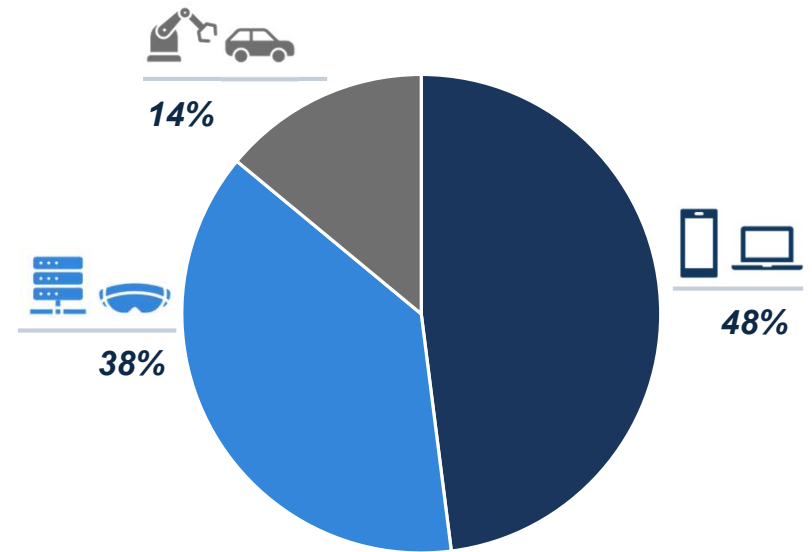


Stabilization of volumes in Consumer market



Softness in Automotive and Industrial

Split by end markets





Financial Highlights

Q4 2025

Revenues were **161.8€m**

up 3.5% YoY, up 15.0% QoQ

Gross Profit was **71.8€m**

up 13.4% YoY, with a margin of 44.4%

Ebitda was **55.3€m**

up 34.2% YoY, with a margin of 34.2%

FY 2025

Revenues were **628.4€m**

up 15.7% YoY

Gross Profit was **279.1€m**

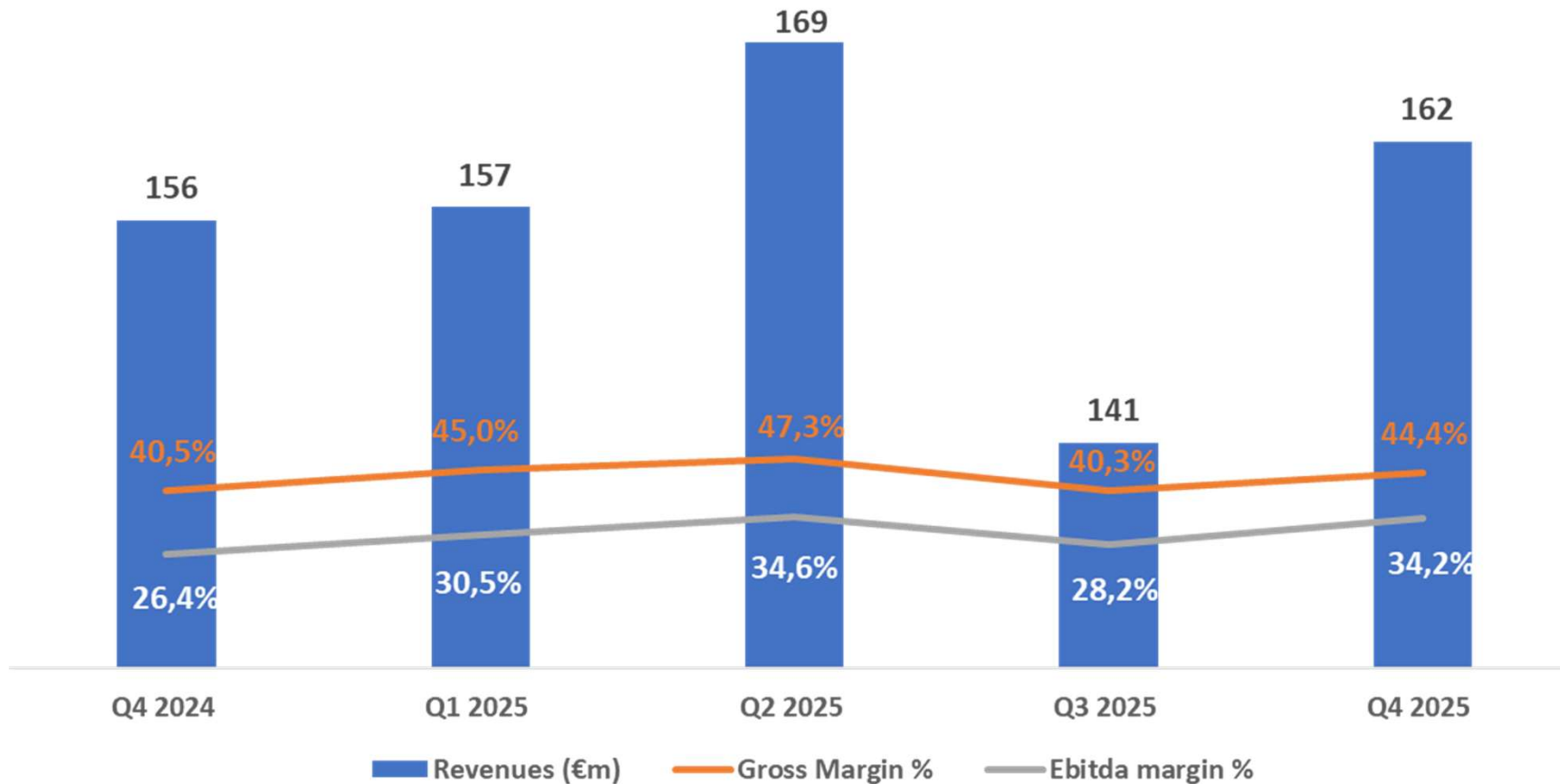
up 24.9% YoY, with a margin of 44.4%

Ebitda was **201.4€m**

up 47.5% YoY, with a margin of 32.1%



Financial Highlights by quarter





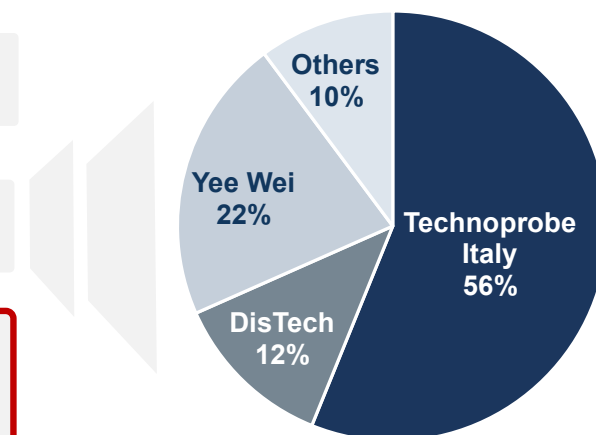
FY 2025 results

	FY 2025	FY 2024	YoY%	Notes
Revenues (€m)	628.4	543.2	+15.7%	<ul style="list-style-type: none"> • Organic growth: rising trend in AI and slight increase in consumer, partially offset by shrinkage in auto and industrial • Change in perimeter (DIS contributed for 12 months in 2025 vs 7 months in 2024) • FX negative impact for €28m
Gross Profit (€m)	279.1	223.4	+24.9%	<ul style="list-style-type: none"> • Recovering in production efficiency • Operating leverage
<i>% margin</i>	44.4%	41.1%	+330 bps	
Ebitda (€m)	201.4	136.5	+47.5%	<ul style="list-style-type: none"> • Ebitda margin benefited, in addition to the above, also from US reorganization positive impact completed in H1 2025
<i>% margin</i>	32.1%	25.1%	+700 bps	
Net Financial Position (€m)	684.2	656.3		<p>Variance mainly attributable to solid cash flow from operating activities (+212€m) and the disposal of Santa Clara building (+26€m), partially offset by the acceleration of Capex (-99€m), the acquisition of a minority stake in Yee Wei Inc. (-20€m) and Innostar Service Inc. (-7€m), together with the treasury shares buy back (-60€m) and the unrealized fx impact on foreign currency bank accounts (-22€m)</p>
	Dec 31, 2025	Dec 31, 2024		



Capex to Support Organic Growth

	FY 2022	FY 2023	FY 2024	FY 2025 E*	FY 2025
€uro/m					
Revenues	549	409	543		628
Capex	84	73	100		99
Capex as % of Revenues	15%	18%	18%	8%-10%	16%



Increased due to acceleration in Q4 of the capacity expansion plan

*Capital Market Day target



2026 market outlook & testing perspective

Geo-Politic Framework

- **Wartime scenario in the Middle East affect worldwide economic stability**
- **Export controls shaping products roadmaps**
- **Supply chain regionalization to offset manufacturing concentration risk**

Market Drivers: Volumes & Test Intensity

Structural growth in:

- **artificial intelligence,**
- **high-performance computing (HPC) and**
- **advanced memory (advanced packaging)**

Volumes

Increasing test demand

Technology

Increasing device architecture complexity which requires more “Known good die” focus

Test Intensity

Higher test intensity across the manufacturing flow

2026 - Agreement in principle to strengthen Chinese market



*TPEG patents, Equipment, Know-how

RATIONALE OF THE AGREEMENT

- ✓ Enhance Technoprobe presence in Mainland China through the development of **TPEG technology**
- ✓ Strengthen the **protection of the Technoprobe Group's know-how and Intellectual Property** in the Chinese market
- ✓ Further expand **customer base**
- ✓ Operations expected to gradually ramp end of 2026 / beginning of 2027

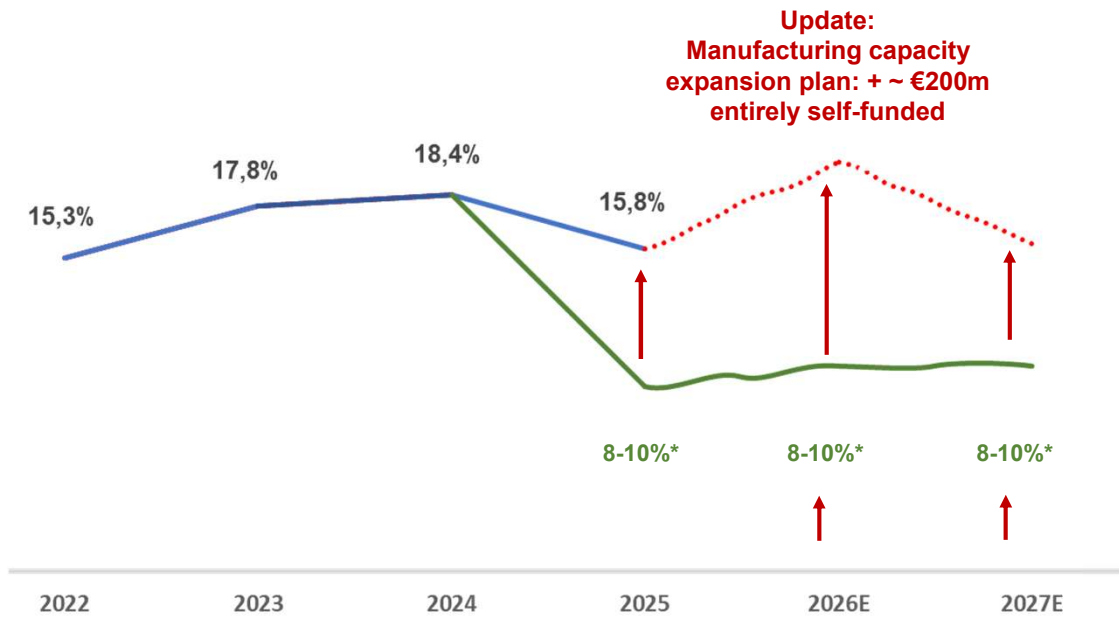
TERMS OF AGREEMENT

- Investment from a Chinese partner of \$35m expected to be implemented through the **subscription of a reserved capital increase to be resolved by DIS China** following which the new partner would hold an equity interest of approximately 30% in DIS China; the execution will in any event **be subject to the obtaining of authorization from the competent Italian authority under Golden Power regulations**, as well as the completion of the required approval process before the relevant Chinese authorities (including the State Administration of Foreign Exchange and the State Administration for Market Regulation), and to certain other customary conditions precedent.
- Incorporation by DIS China of **an operating subsidiary** in the Suzhou area, which will be entrusted with the **manufacturing and distribution** of TPEG-based products
- Agreement, reached in its essential terms, **will be formalized by the end of March** through the execution of the relevant definitive agreements.

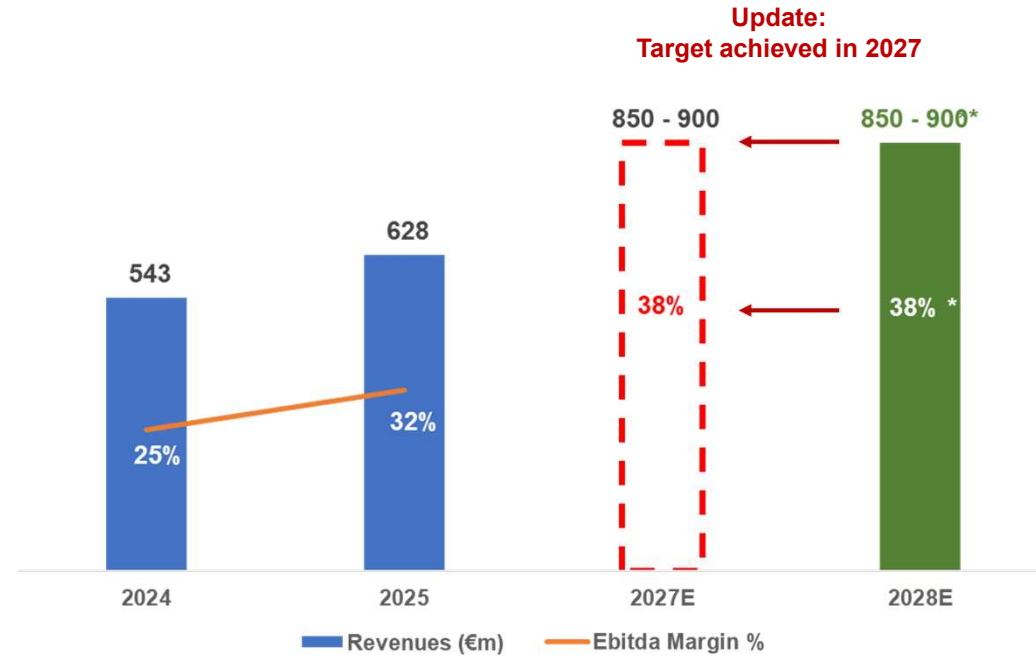


Mid-Term Trend Update

Capex on Revenues Update



Revenues – Ebitda target Update



*Capital Market Day target



Q1 2026 Guidance

Revenues: 182€m

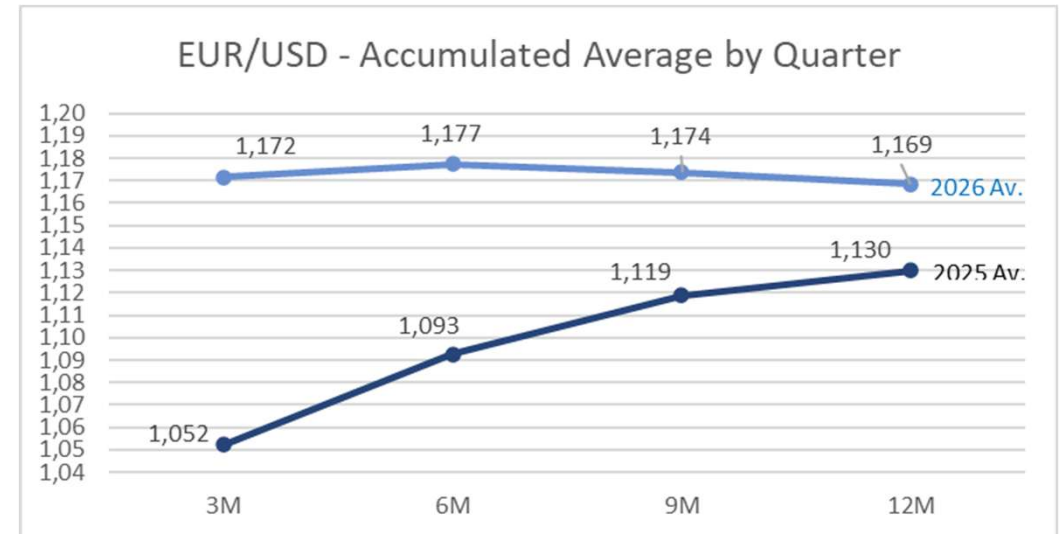
(+/-3%)

Gross Margin: 46.5%

(+/-200bps)

Ebitda Margin: 35.4%

(+/-200 bps)



Average	Q1 '25	Q2 '25	Q3 '25	Q4 '25	Average *	Q1 '26	Q2 '26	Q3 '26	Q4 '26
	1,052	1,134	1,168	1,163		1,172	1,183	1,167	1,153
3M	1,052					1,172			
6M		1,093				1,177			
9M			1,119			1,174			
12M				1,130		1,169			

*Estimate