Technoprobe S.p.A.
Mediobanca Mid Cap Conference 2026

January 22, 2026

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Innovation begins with us

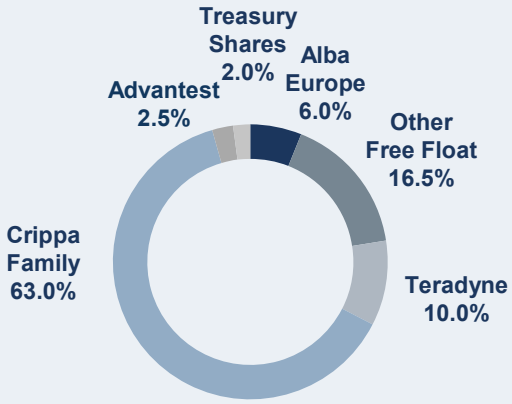
A leading company in the field of semiconductors and microelectronics

Company Overview

2024 Key financial metrics

Revenue	Ebitda	Net Income	Net Financial Position	Mkt Cap
€543.2m **+22%** CAGR 19-24	**€136.5m** **25%** EBITDA margin	**€62.8m** **12%** on revenues	**€656.3m** as at 12/31/2024	**~€10,3bn** as at 1/21/2025

Shareholding Structure

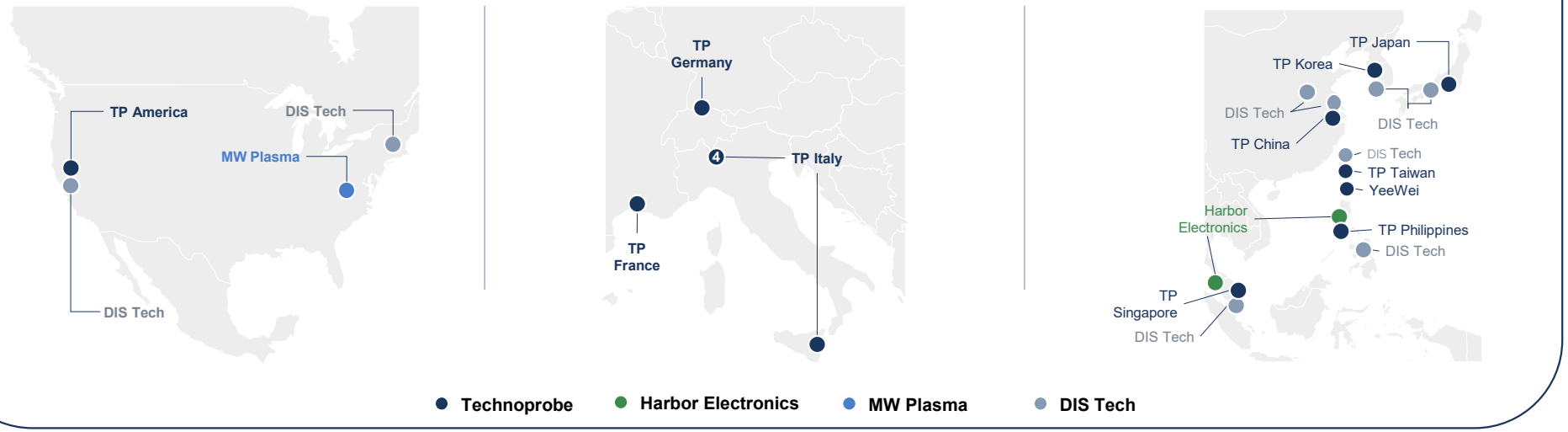


- Leading player in designing and manufacturing of **probe cards to test Logic chips**
- Manufacturing process **vertical integrated**
- Strong focus on **innovation**
- Extensive **global presence** and widespread **local footprint**

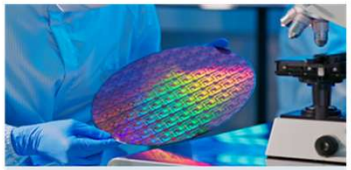
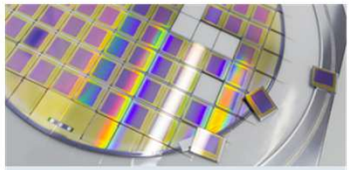
Where we are

Headquartered in Italy with branches in Europe, America, and Asia

>3.3k Employees ***3 Continents*** ***10 Countries*** ***23 Legal Entities***

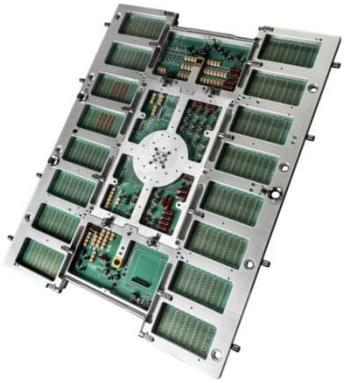


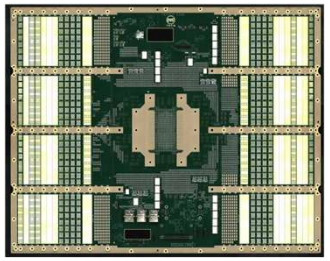
Probe Cards in the semiconductor manufacturing process

FRONT END		BACK END		
Wafer fabrication & pre-assembly preparation	**Wafer Testing Level**	Wafer dicing	Assembly & Packaging	**Final Testing Level**
				
Construction of the integrated circuits (dies) that compose the wafer.	Wafer's dies testing for functional defects through probe cards. **Technoprobe focuses on Vertical MEMS.**	Wafer separation into individual dies, ready for subsequent assembly.	Individual die enclosure in a protective package ready for final testing and shipment.	Chip final testing with burn-in or test sockets. **Technoprobe focuses on Pogo Pin for test sockets.**

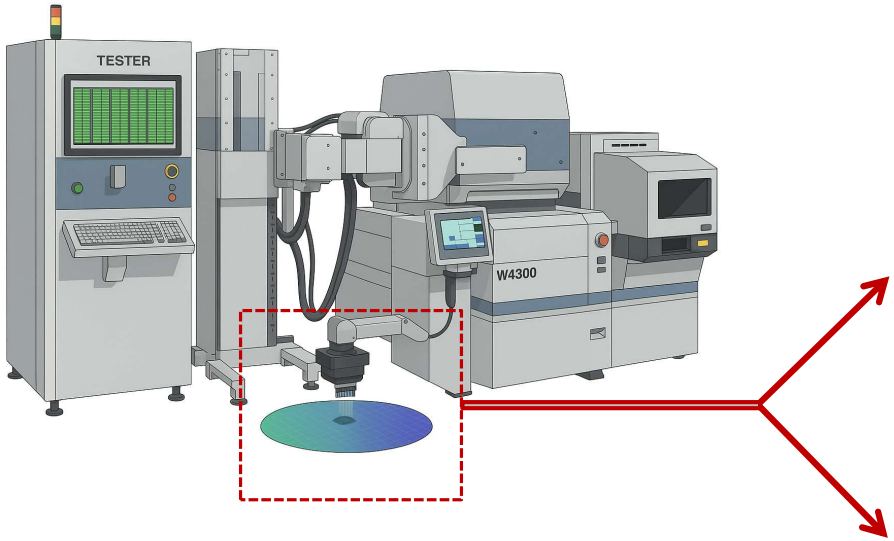
Our positioning in the testing space

FRONT END		BACK END		
Wafer fabrication & pre-assembly preparation	**Wafer Testing Level**	Wafer dicing	Assembly & Packaging	**Final Testing Level**
	Wafer Level			Socket
	Singulated Die			System Level Testing
	Advanced Packaging			
	Probe Card			**Device Interface Board**





The testing phase

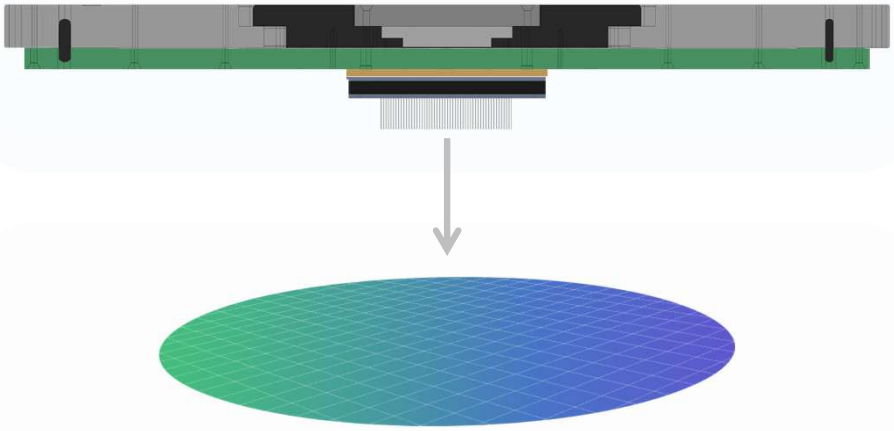


Tester (ATE)

- A tester, or Automated Test Equipment (ATE), applies electrical signals to semiconductor devices and measures their responses to verify performance and functionality
- ATE systems execute test programs to identify manufacturing defects and ensure chips meet design specifications

Probe Card

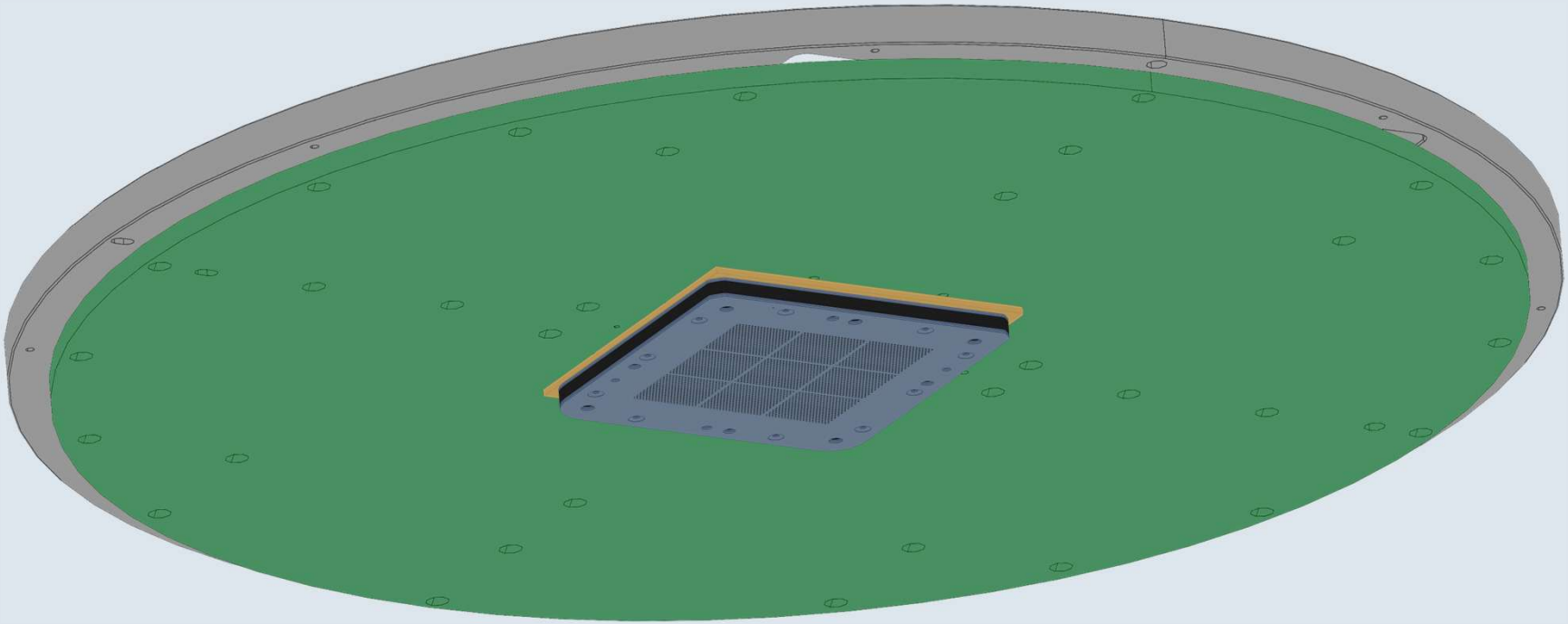
- A probe card is a precision device with microscopic needles or MEMS tips that make electrical contact with each die's test pads on the wafer
- The probe card connects the tester (ATE) to the wafer, enabling parallel testing of multiple dies before they are diced into individual chips



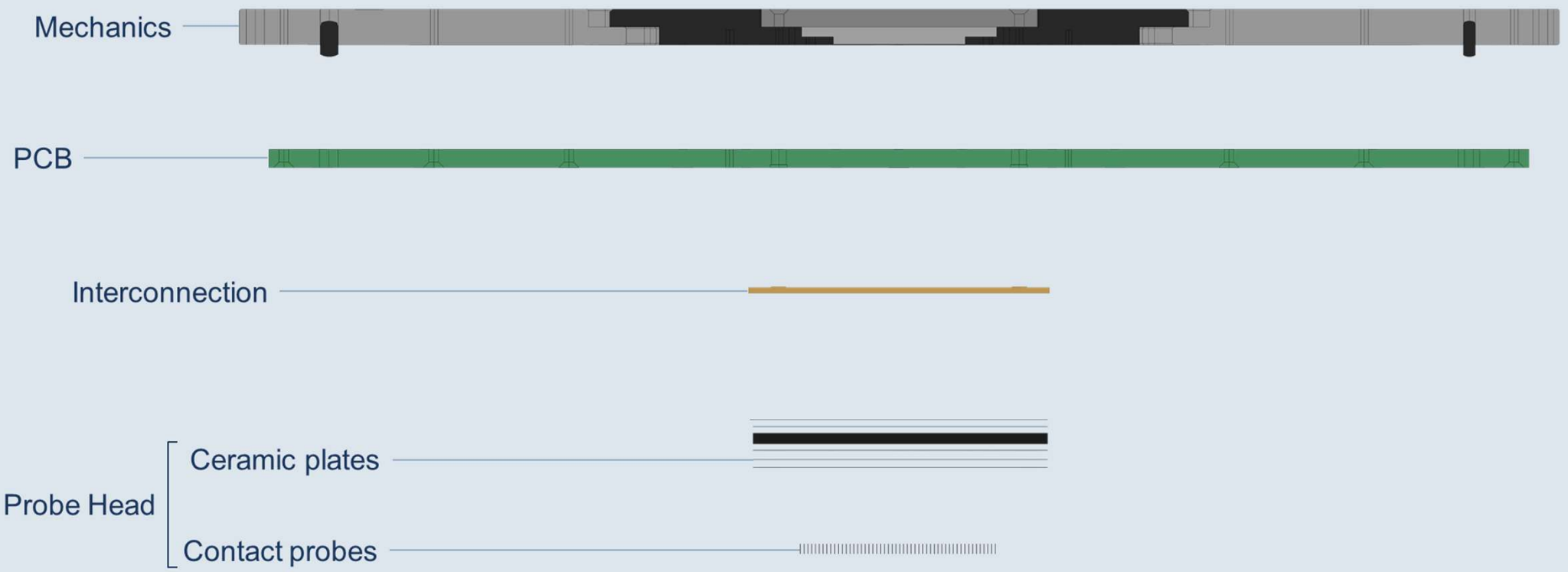
Wafer

- A wafer is a thin, circular semiconductor substrate (most commonly silicon) on which integrated circuits (dies) are fabricated
- Each die functions as an individual integrated circuit that, once separated (diced) and packaged with external connectors, becomes a finished semiconductor chip

The Probe Card

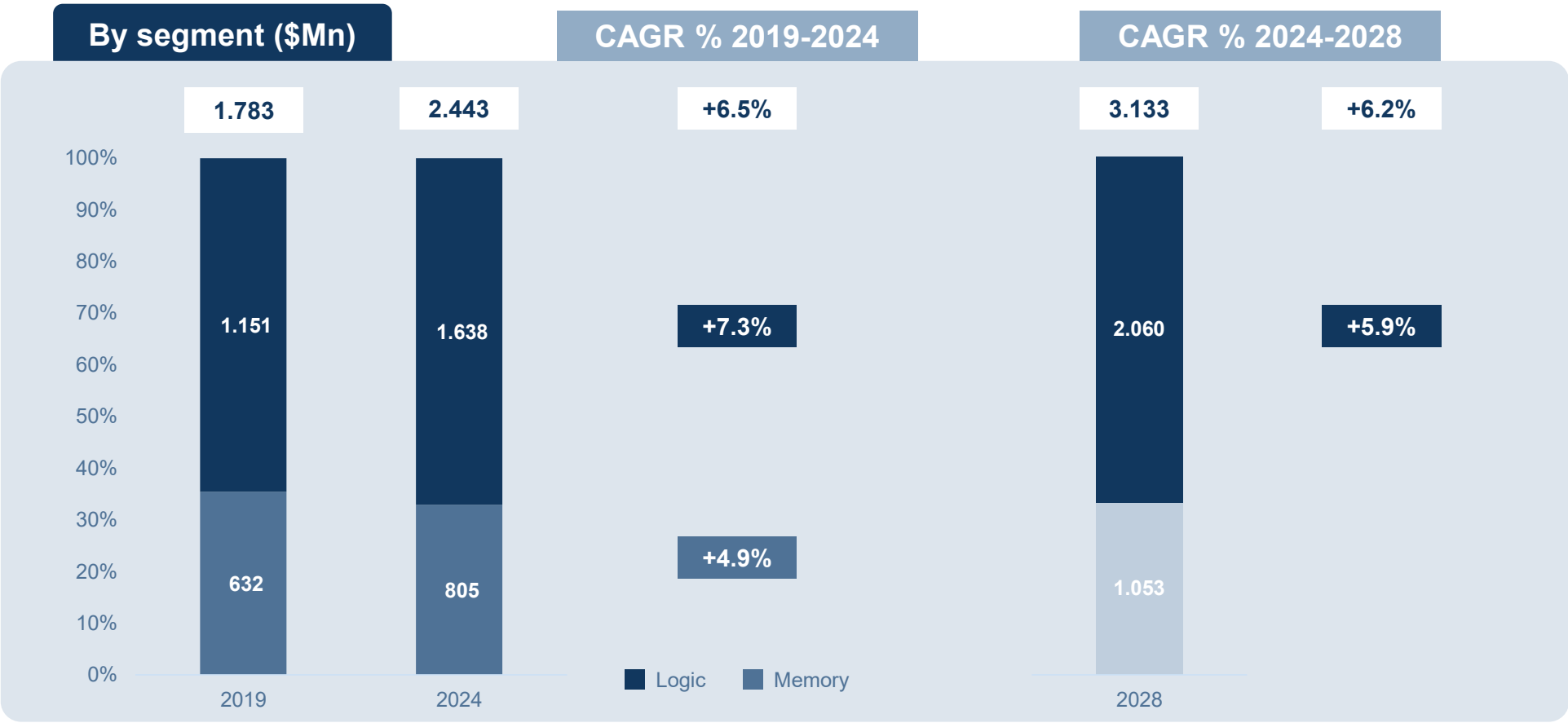


The Probe Card



Reference Market

Overview of the Semiconductor Probe Cards market

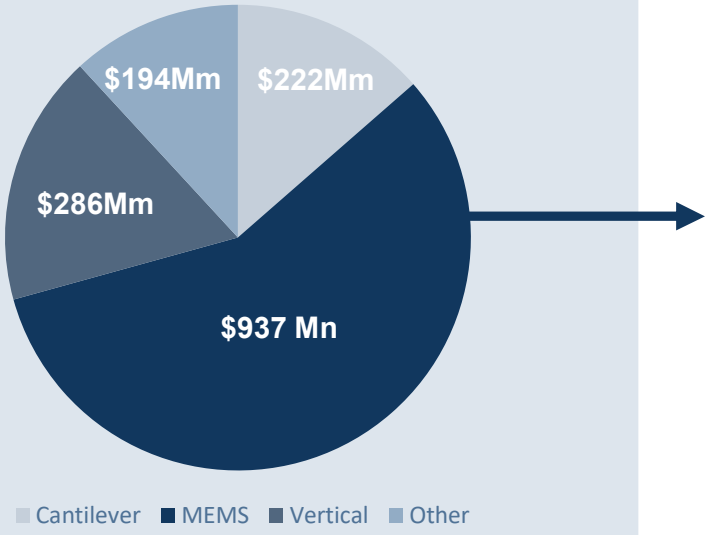


Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures. Memory: DRAM+NVM & Other memory. Logic: MEMS, Power, RF, CMOS Image Sensors, Photonics, Other non-memory, WAT.

Our reference market

2024 Logic Probe Card market

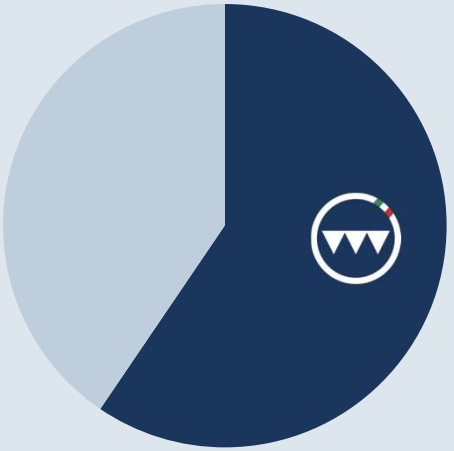
$1,6 Bn



Market Share: 34%

2024 MEMS Logic Probe Card

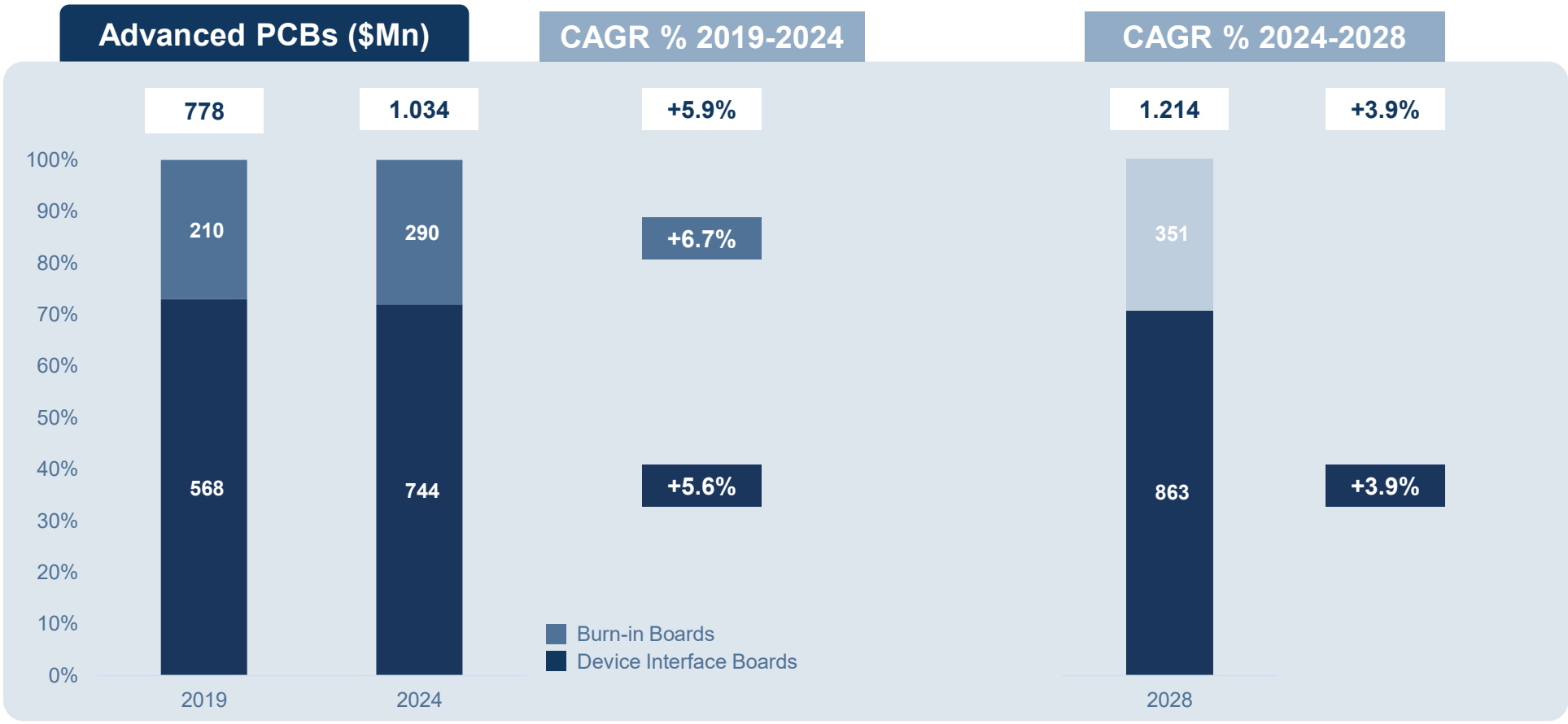
$937 Mn



Market Share: 60%

Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.

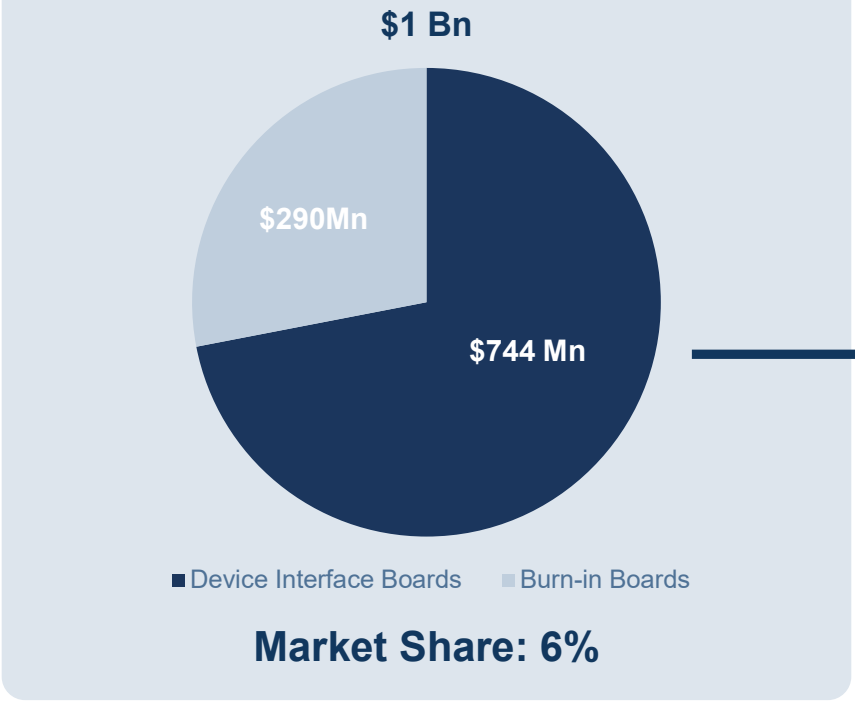
Final Testing market – Advanced PCBs



Source: Yole Test Interface Board market monitor Q3 2024 (Sept.2024) – rounded figures.

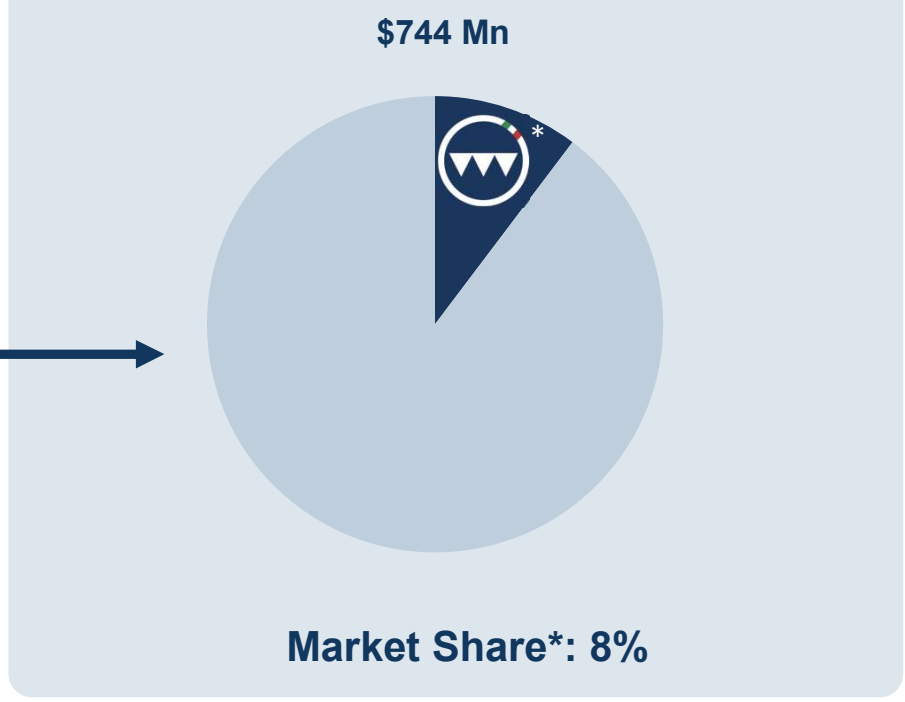
Final Testing market – Our reference market

2024 Advanced PCB for semiconductor



Market Share: 6%

2024 Final Test DIB market



Market Share*: 8%

Source: Yole Test Interface Board market monitor Q3 2024 (Sept.2024) – rounded figures.
(*) Based on DIS Tech Final Test FY24 data. Company acquired by Technoprobe on May 27, 2024.

Business Model

INNOVATION BEGINS WITH US

A successful and vertically integrated business model

		Design	Manufacturing	Assembly
Wafer Testing Level				
Mechanics		✓	✓	✓
PCB		✓	Manufacturing partners & other suppliers	✓
Interconnection		✓	✓	✓
Probe head Ceramic plates Contact probes		✓	✓	✓
Final Testing Level				
Device Interface Boards		✓	Manufacturing partners & other suppliers	✓

Supported by an open eco-system partnerships

TERADYNE

Accelerate growth of complete Probe Card and Final Test Interfaces by acquisition of DIS

Joint Development Projects to deliver superior customer value in SOC and Memory

TECHNOPROBE

ADVANTEST

Priority suppliers of PCB

Joint Development Projects to share knowledge

The Probe Card manufacturing process

Probe unit

Production of probes leveraging a highly innovative and proprietary technology on **Ceramic Plates** of the **Probe Heads**

Probe head unit

Production of the **Ceramic Plates** on which Probes are then assembled

Assembly of Ceramic Plates with the probes produced in the Probe Unit

Printed Circuit Board (PCB)

Partially outsourced

Board unit

Welding and connection of the Multi Layer Organic (MLO) to the Printed Circuit Board (PCB)

Subsequently, connection of Board component (MLO and PCB welded together), with the Probe Head

Certificate unit

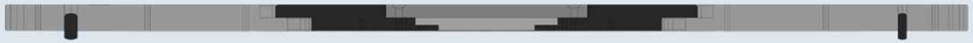
Final quality testing of the mechanical and electrical features of assembled probe card

Substrate Unit

Multi Layer Organic (MLO)

Mechanical Shop

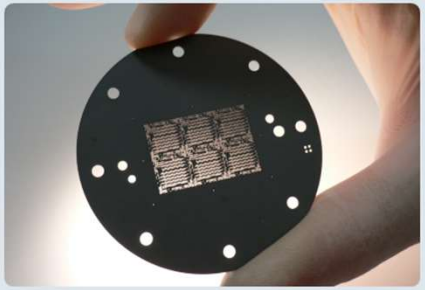
- Production of the mechanical elements used across all stages of the probe card manufacturing process
- The unit is also engaged in the production of highly innovative and customized machines, not available on the market, used in the production process



The wide range of highly innovative technologies inside

Advanced micromachining

Advanced laser cutting:
high accuracy and fast lead time

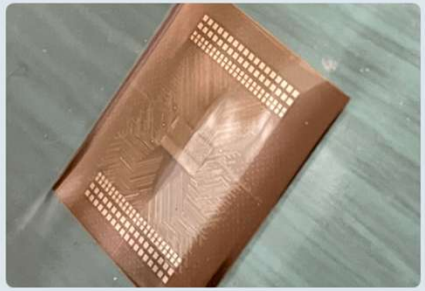


Thin film

Strong investment in advanced thin film technology to reduce lead time and improve quality and complexity

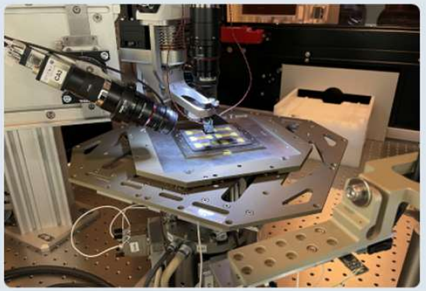
3D MEMS

Acquisition of MICROFABRICA in 2019; the sole company in the world specialized in 3D metallic MEMS manufacturing



Advanced manufacturing

Advanced manufacturing for high volume and best quality assembly of micro components

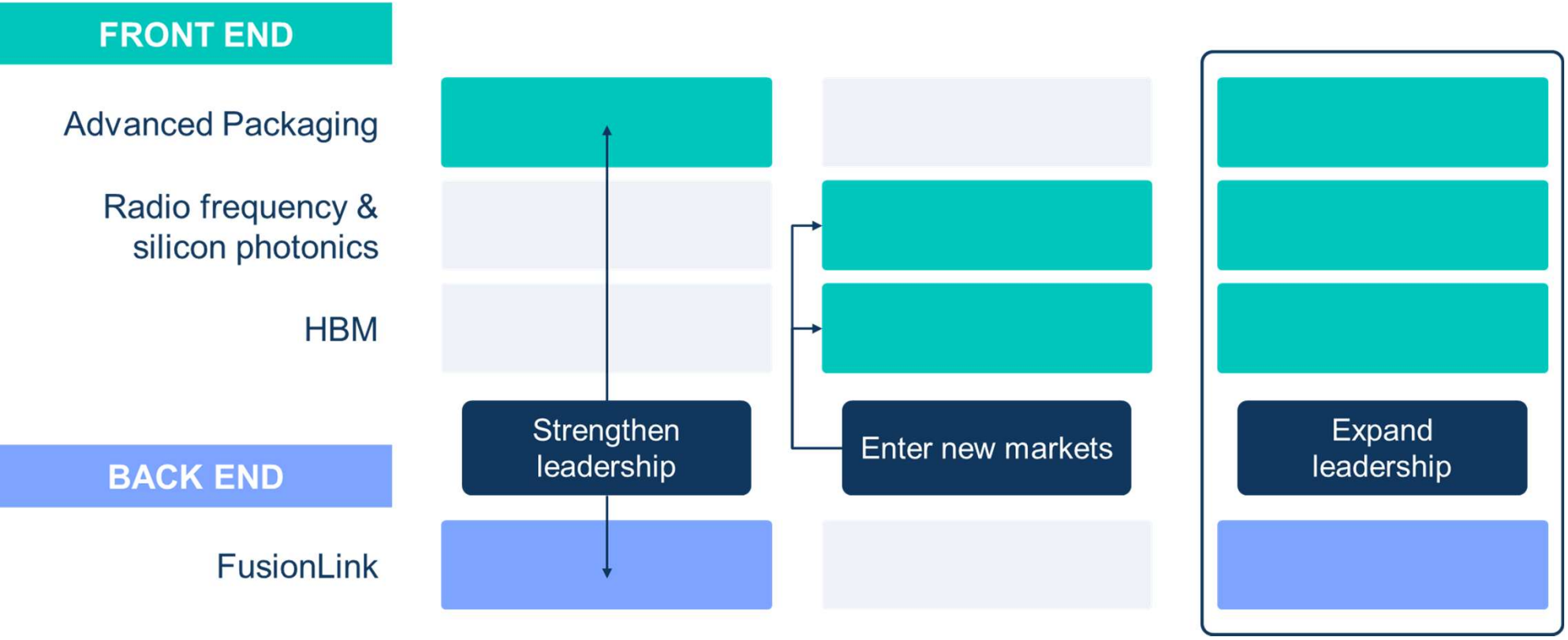


Vision & Strategy

Challenges & strategic setting

1	**Evolution of chip technology (more than Moore)** Scaling slow down as enabler for **chiplets**, **3D architectures** and **new materials**	→ **Continuous investments in R&D** → **M&A as accelerator of technological development**
2	**Increase in complexity** **Design and manufacturing** are becoming essential capabilities to reliably deliver **complex solutions**	→ **Strategic partnerships** → **Vertical integration of the most value-added components of the probe card**
3	**Client satisfaction** **Reliability** of the product & **on-time delivery**	→ **Support on site** → **Commercial agreements**

Growth drivers & trajectories



Technoprobe as advanced packaging enabler

Fine pitch and ultra – large pin count
Necessary to effectively probe HPC and HBM's and all leading-edge product

High-speed
Short, ultra short and RF-specific needles technology to manage high speed interconnect IO, including SiPh

High power and thermal

- Delivering high power to DUT in effective and reliable way
- Ability to remove heat dissipated by the probe card (directly or because of power transferred from DUT to PC)

High-density interconnect
Ultra-high complexity PCB and MLO/MLC for resource fan-out on ATE/SLT

A hungry world of wideband applications

Exponential increase in number & type of connected things

Increasing reliance on the cloud

Bandwidth-hungry applications

Analog radio frequency

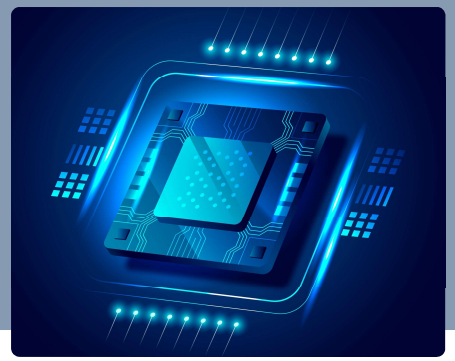
Satellite communications and sensing, automotive radar, mobile communication,…

Chiplet probing

High density and high-speed IO inside chiplet demand for high-performance probe needles

Silicon photonics

Chiplet to chiplet interconnect / photonics-driven computing



FRONT END Proliferate radio frequency and silicon photonics

Technoprobe silicon photonics testing solution

Fine pitch probing
align with advanced packaging roadmap

Technoprobe IP
usage of standard wafer prober

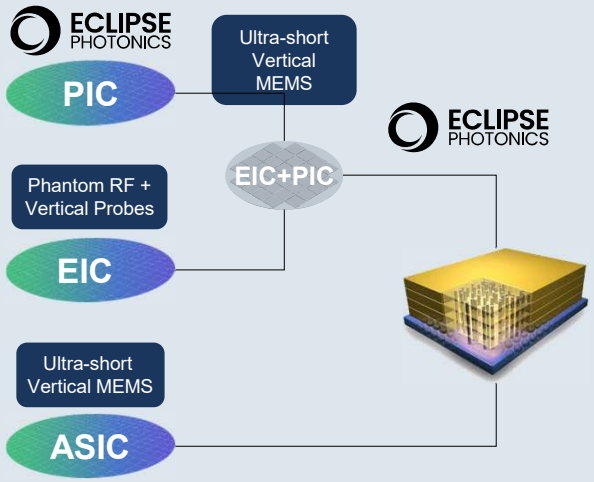
Radio frequency probes
high-speed performances in same probe card solutions

Integration of other IP from specific segment suppliers
flexibility and compliancy with customer preferred test method

Eclipse photonics

Where it applies

Wafer level | Reconstituted wafer level | Optical Engine



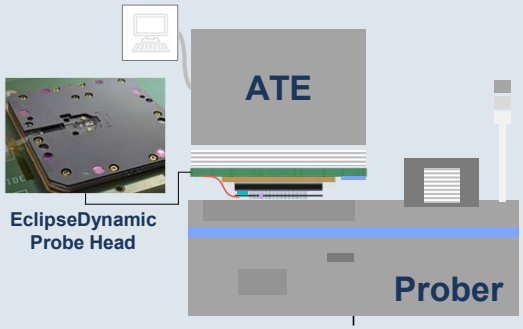
From the PIC to the optical engine

- EclipsePhotonics can probe optical funtion at more levels
- The test interface can be designed for DC, AC and functional test/System Level Testing
- Can be integrated with multiple automation solutions

How it works

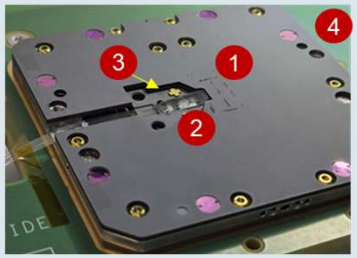
An autonomous instrument

- EclipsePhotonics embeds the electronics to autonomously operate when on the tester
- It integrate a programmable unit to execute the alignment algorithm(s), interface to the tester and operate the electronics
- The integration with ATE gives the capability to control the instrument from the user test program



Shop-floor preferred wafer prober

What it delivers



Probe card content

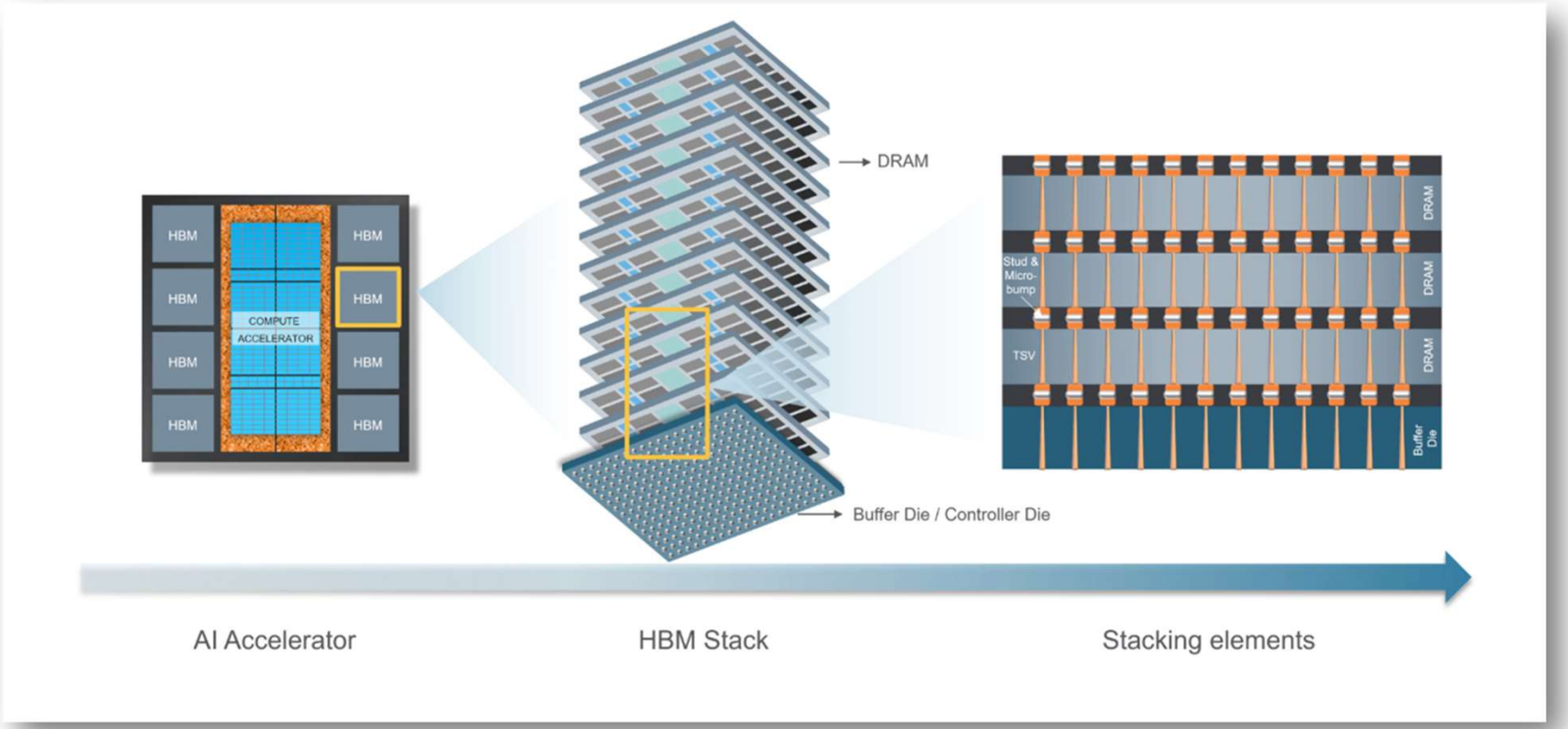
1. Vertical MEMS needle and Phantom RF probes
2. FAU, fiber optics and optical connector (blind mated)
3. FAU positioner (up to 6-axis)
4. Electronics to activate and control the positioner

What it delivers

- Direct docking
- Integrated optical and electrical probe, with off-line card certification
- High operation stability, repeatability and immunity to external factors
- In-field repairability
- Minimal optical to electrical pin distance constraints

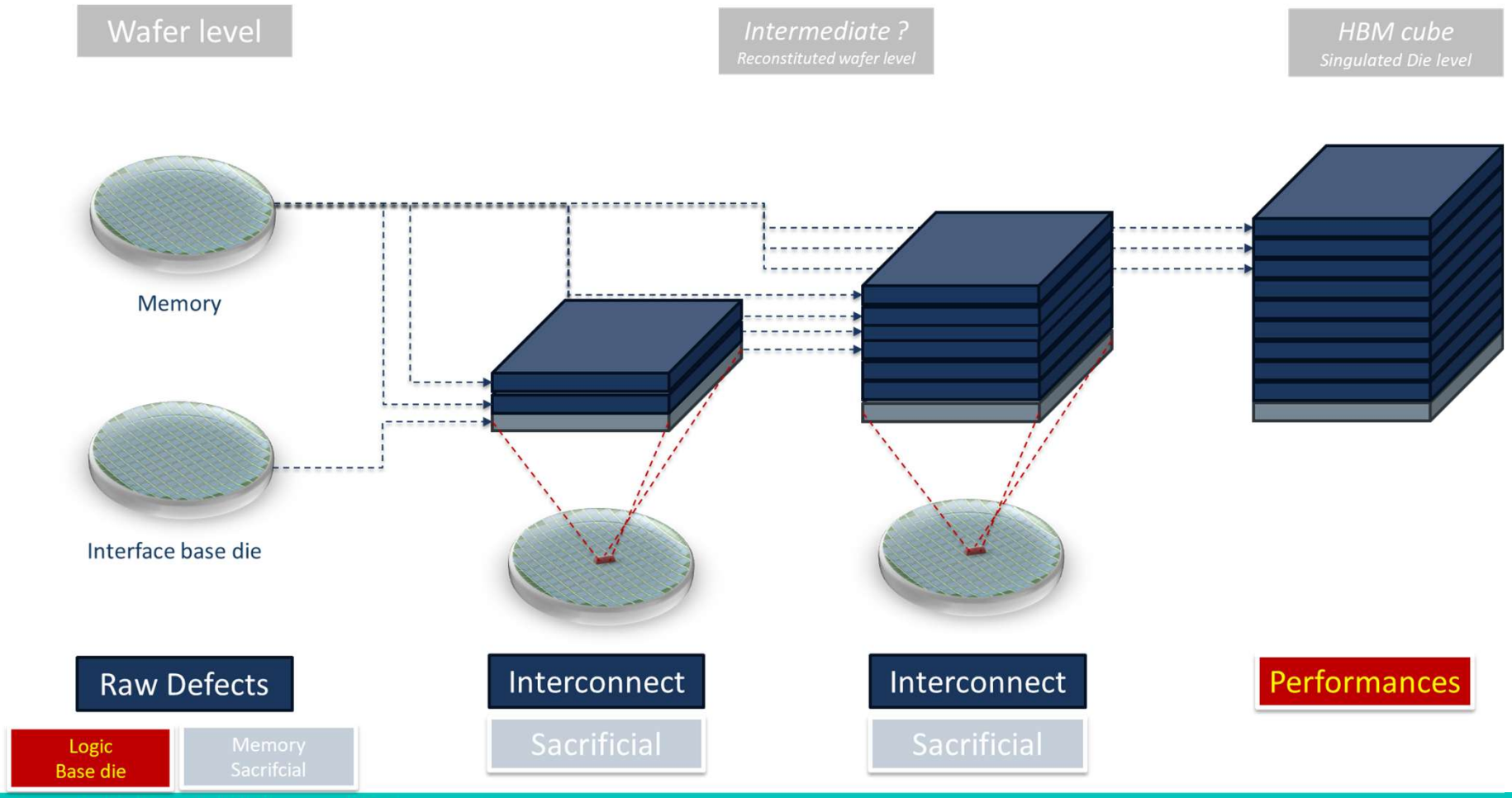
***PIC**: photoncs integrated circuit* ***EIC:** eletronic integrate circuit* ***ASIC:** Application-Specific Integrated Circuit*

HBM Architecture



Cartoon credit: Applied Material web site

HBM Test Flow



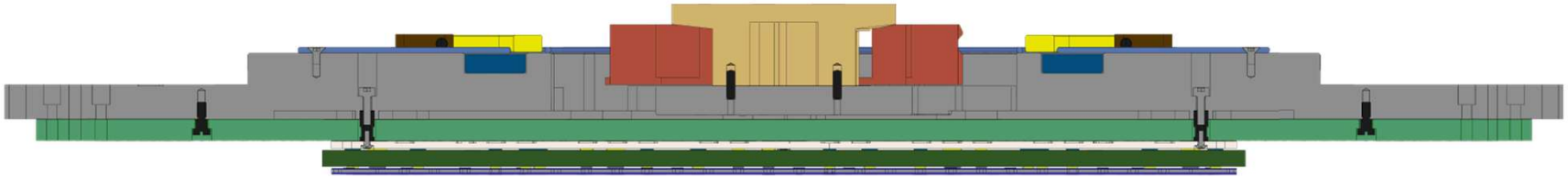
FRONT END Enter the High Bandwidth Memory (HBM) segment

HBM: new testing solution

DRAM and HBM are typically tested with **microcantilever** probing technologies.

Most **advanced HBM** and Next Generation products are becoming more challenging in terms of pad pitch, signal integrity, and power.

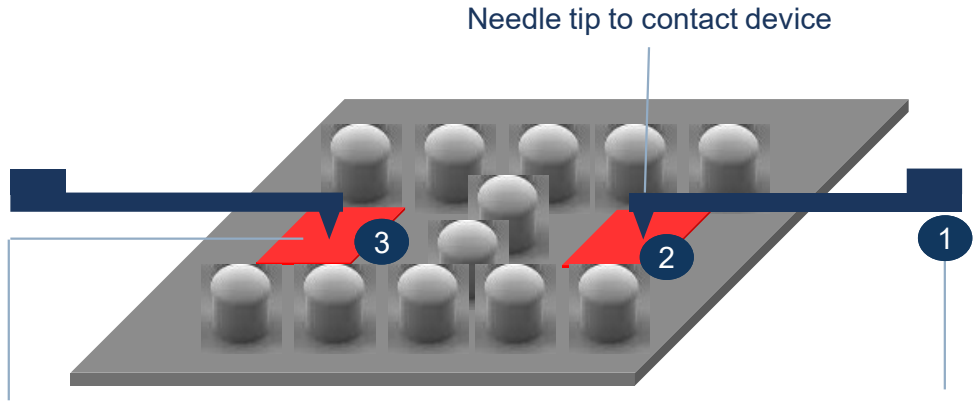
For both applications Technoprobe is leveraging on **Vertical MEMS** solution and on a unique PC architecture.



HBM Test Flow: microcantilever technology

Microcantilever

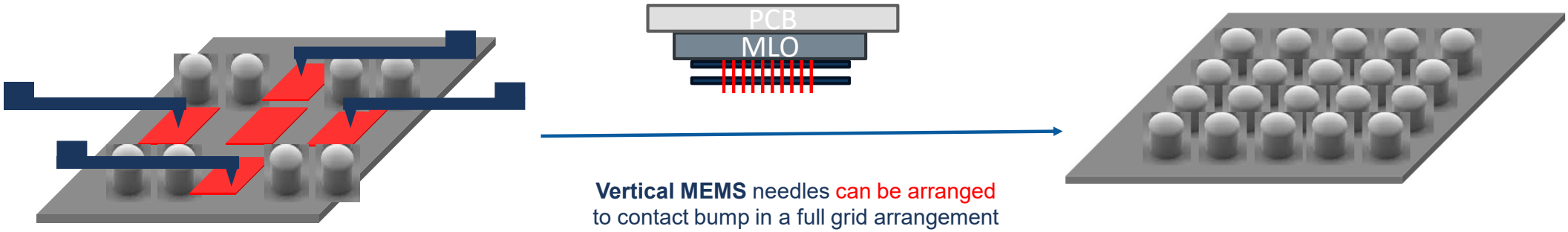
needles cannot be arranged to contact bump in a full grid arrangement



Sacrificial pads are necessary to enable usage of microcantilever

microcantilever end point which shall be soldered to a PCB/MLC

HBM Test Flow: vertical mems vs. microcantilever



Vertical MEMS needles can be arranged
to contact bump in a full grid arrangement

FusionLink

FUSIONLINK
Innovate • Optimize • Accelerate

FusionLink is an advanced interface architecture that combines the best manufacturing technologies & processes to redefine what's possible for test strategy

- FusionLink unifies the know-how across probe cards and device interface boards under one architectural framework

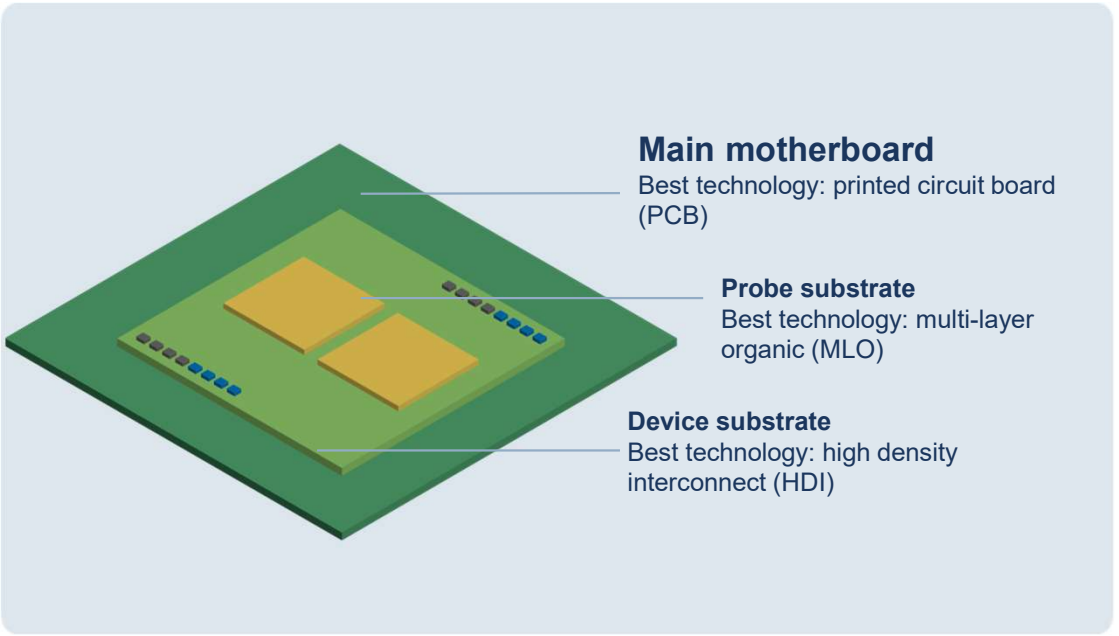
The Best Performance

- FusionLink brings together the latest advances in semiconductor packaging and high-performance materials with Technoprobe's proprietary innovations in design, fabrication, assembly, and verification

The Highest Quality

- The architecture is not a "one size fits all" but is meant to be optimized per project

Faster Time to Market



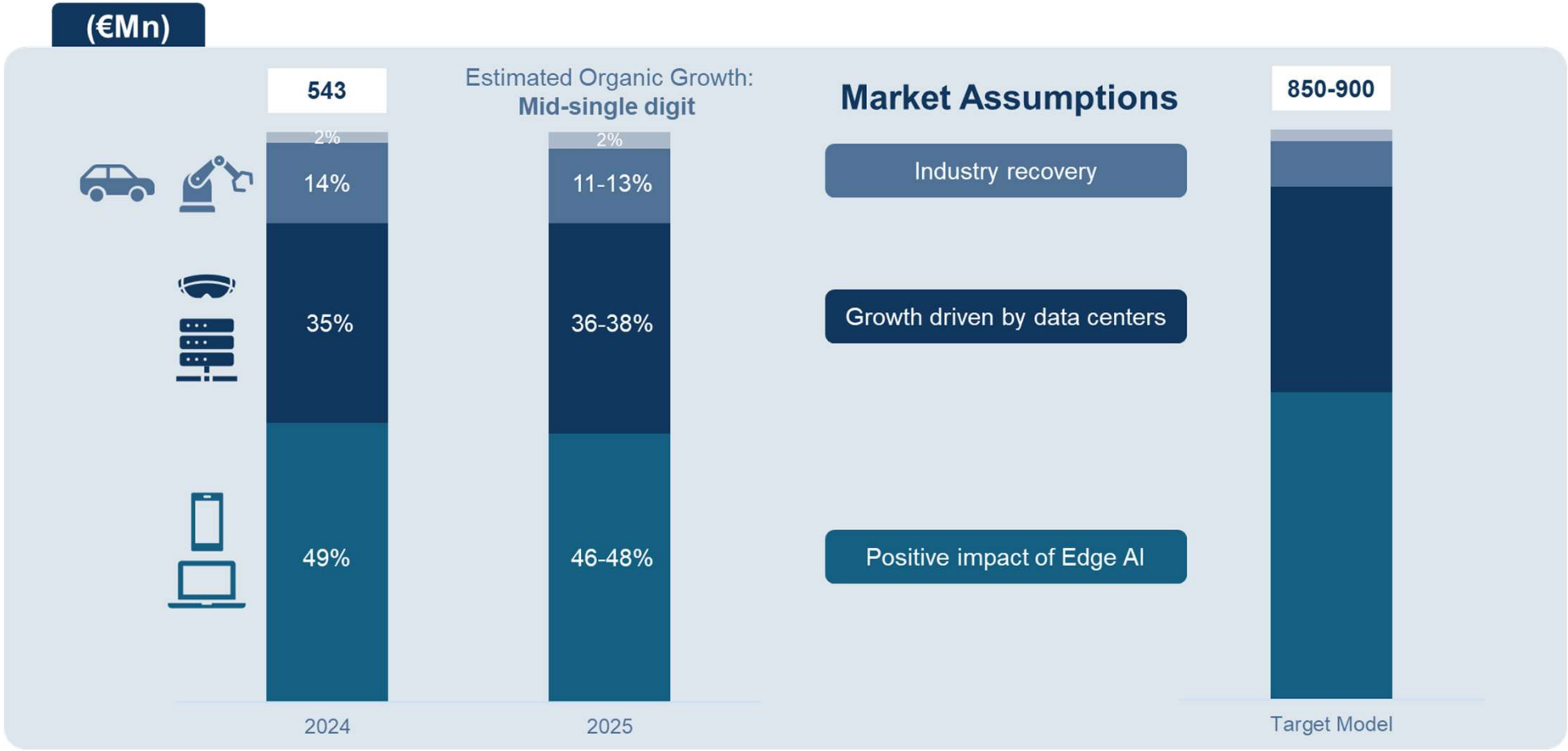
Financial Outlook

Mid-terms scenario

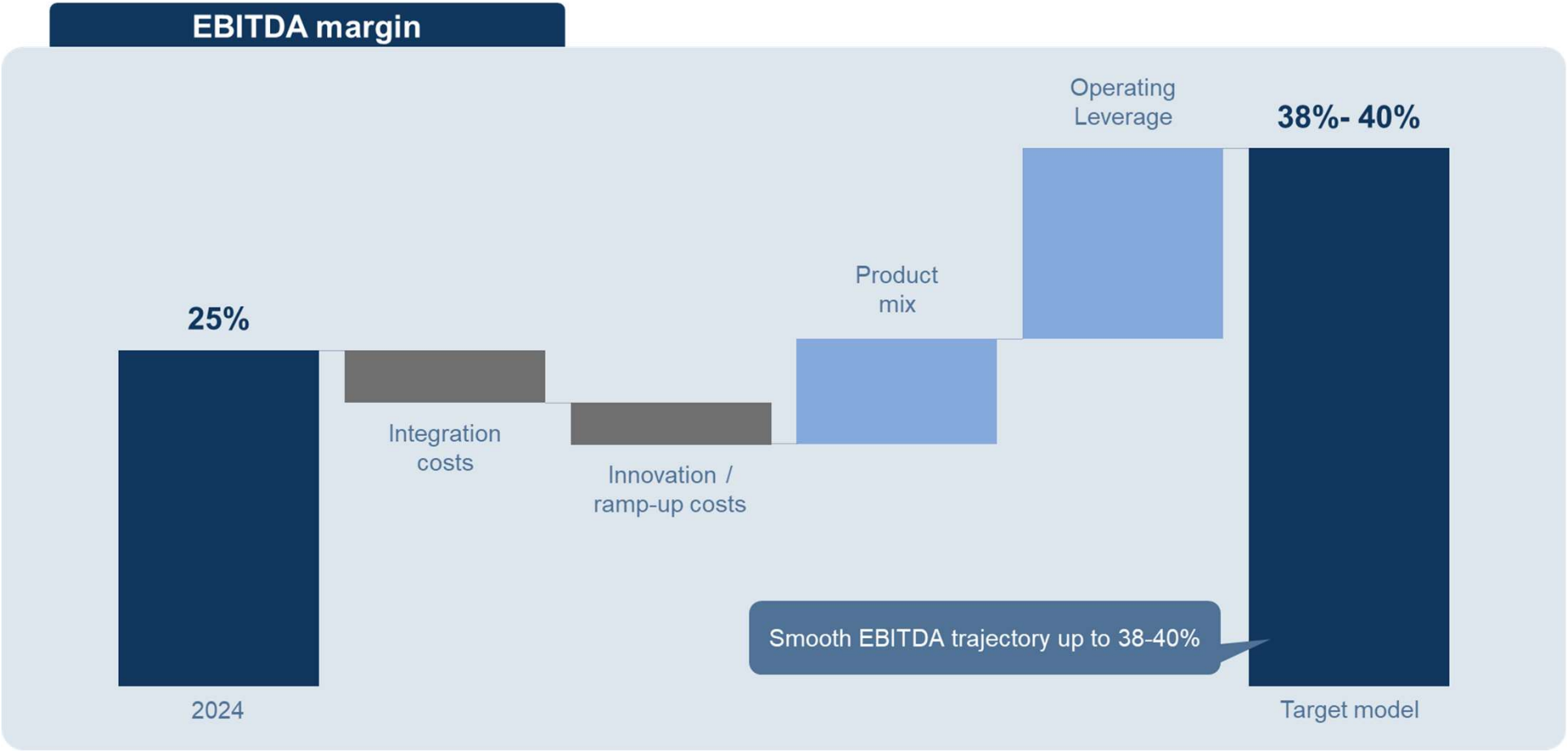
1	**Technological complexity evolution**	→ Testing solution for Advanced Packaging → Increase in demand for high-precision tests
2	**Market trends**	→ AI will lead the growth for many market segments → Expansion of memory semiconductor segments
3	**Geo-political instability**	→ Technological sovereignty → Commercial policies

Market trends & revenues path

Market trends & revenues path



Profitability profile



9M 2025 market drivers

Revenues at **466.6€m**

down 16.6% QoQ
up 20.6% YoY


Consistent growth in AI


Slight increase in Consumer market


Softness in Automotive and Industrial

Financial Highlights

Q3 2025

Revenues were **140.7€m**
down 3.5% YoY, down 16.6% QoQ

Gross Profit was **56.7€m**
down 4.6% YoY, with a margin of 40.3%

Ebitda was **39.8€m**
up 15.0% YoY, with a margin of 28.2%

9M 2025

Revenues were **466.6€m**
up 20.6% YoY

Gross Profit was **207.3€m**
up 29.5% YoY, with a margin of 44.4%

Ebitda was **146.1€m**
up 53.3% YoY, with a margin of 31.3%

9M 2025 results

	9M 2025	9M 2024	YoY%	Notes
Revenues (€m)	**466.6**	**386.9**	***+20.6%***	• **Organic growth**: rising trend in AI and slight increase in consumer, partially offset by shrinkage in auto and industrial • **Change in perimeter** (DIS contributed for 9 months in 2025 vs 4 months in 2024) • **FX negative impact** for €12m
Gross Profit (€m)	**207.3**	**160.1**	***+29.5%***	• **Recovering in production efficiency** • **Operating leverage**
% margin	*44.4%*	*41.4%*	*+300 bps*	
Ebitda (€m)	**146.1**	**95.3**	***+53.3%***	• **Ebitda margin benefited,** in addition to the above, also from US reorganization positive impact, terminated in H1 2025
% margin	*31.3%*	*24.6%*	*+670 bps*	

	9.30.2025	12.31.2024	
Net Financial Position (€m)	**665.7**	**656.3**	**Variance mainly** attributable to solid **cash flow from operating** activities (+114€m) and the disposal of Santa Clara building (+26€m), partially offset by **Capex** (-51€m), the acquisition of a **minority stake in Yee Wei Inc**. (-20€m) and **Innostar Service** Inc. (-7€m), together with **shares buy back program** (-32€m) and **the unrealized fx impact** on foreign currency bank accounts (-23€m)

Q4 2025 Guidance

Revenues: 160€m

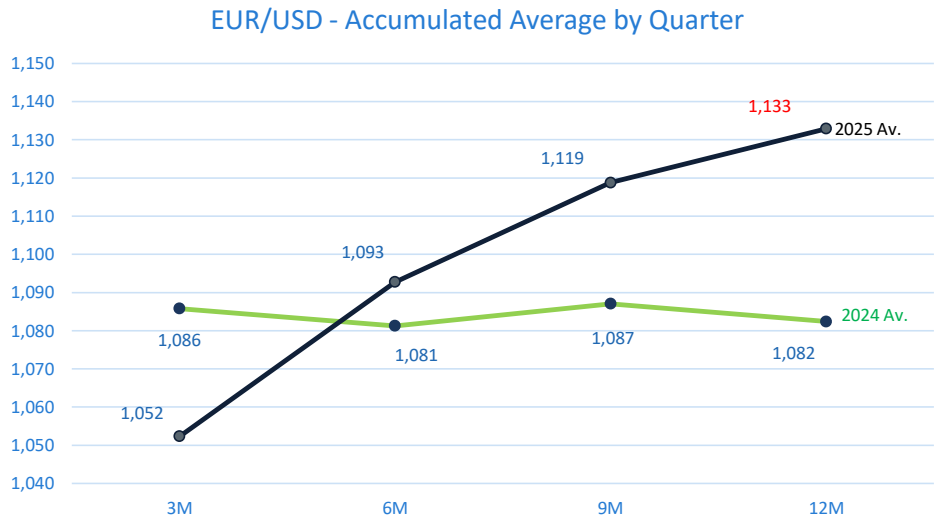
(+/-3%)

Gross Margin: 46%

(+/-200bps)

Ebitda Margin: 34.7%

(+/-200 bps)



Average	Q1 '24	Q2 '24	Q3 '24	Q4 '24
	1,086	1,077	1,098	1,068
3M	1,086			
6M	1,081			
9M	1,087			
12M	1,082			

Q1 '25	Q2 '25	Q3 '25	Q4 '25*
1,052	1,134	1,168	1,175
1,052			
1,093			
1,119			
1,133			

**Estimate*