



**dbAccess European TMT Conference
Technoprobe S.p.A.**

Sept. 4, 2025



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Innovation begins with us

A leading company in the field of semiconductors and microelectronics



INNOVATION BEGINS WITH US

Company Overview



2024 Key financial metrics

Revenue	Ebitda	Net Income	Net Financial Position	Mkt Cap
€543.2m +22% CAGR 19-24	€136.5m 25% EBITDA margin	€62.8m 12% on revenues	€656.3m as at 31/12/2024	~€4,4bln as at 1/9/2025

Shareholding Structure



Leading player in designing and manufacturing of **probe cards**



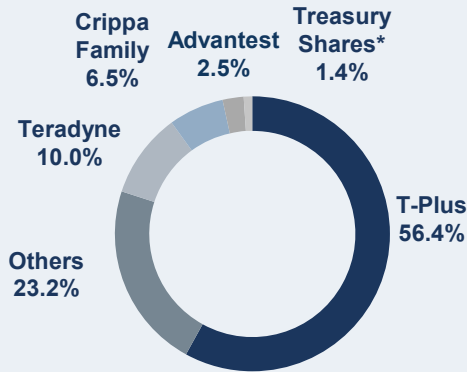
Manufacturing process **vertical integrated**



Strong focus on **innovation**

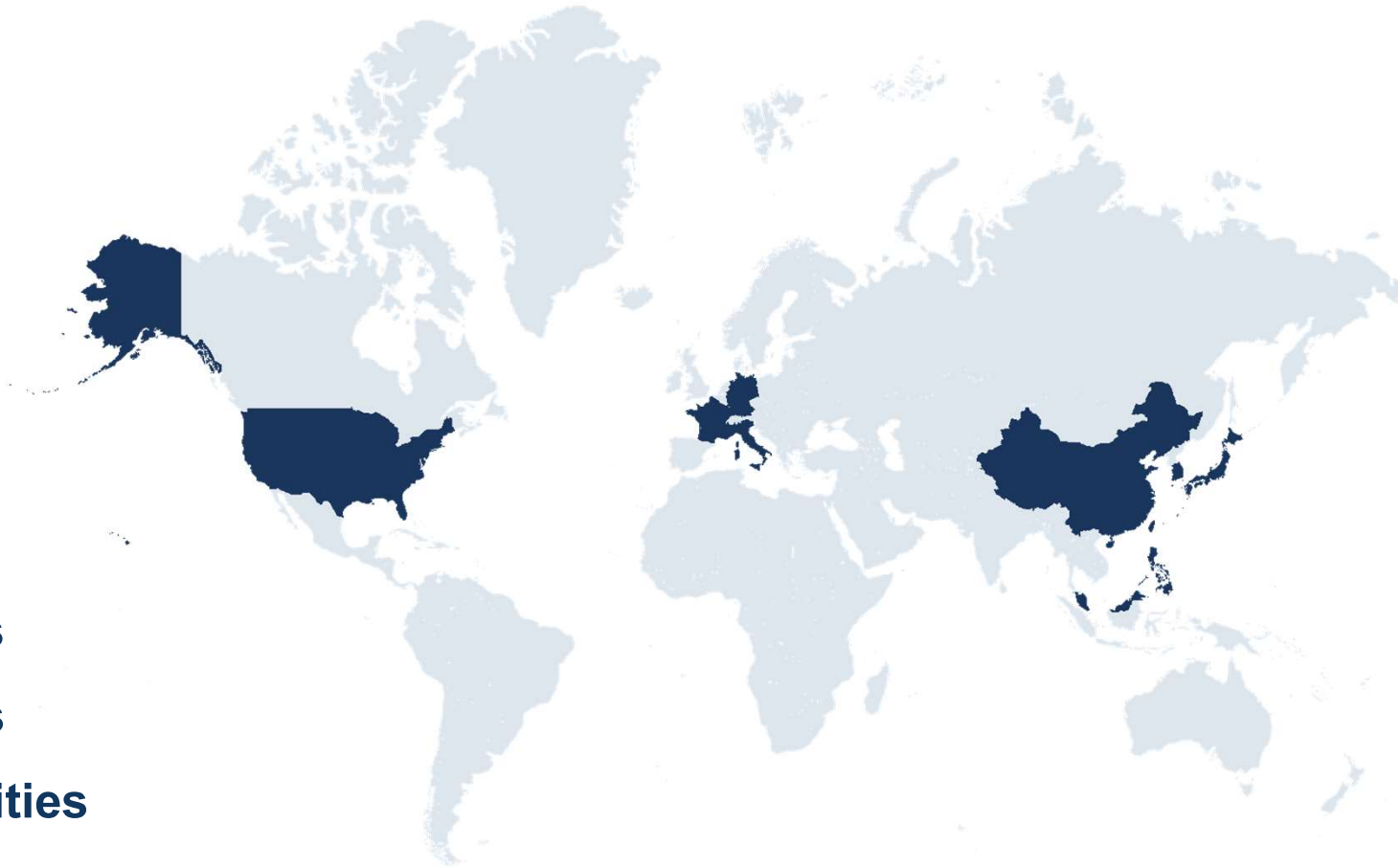


Extensive **global presence** and widespread **local footprint**



*as at August 29, 2025.

Where we are



3 Continents

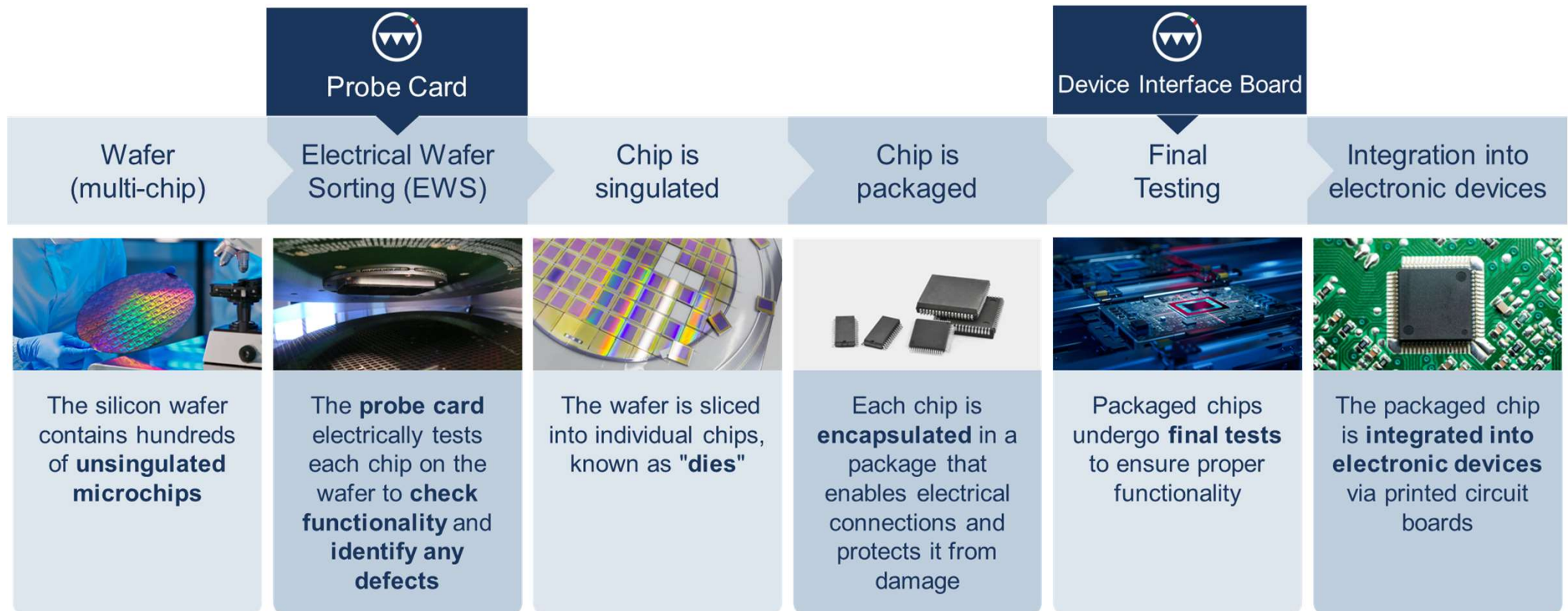
10 Countries

23 Legal entities

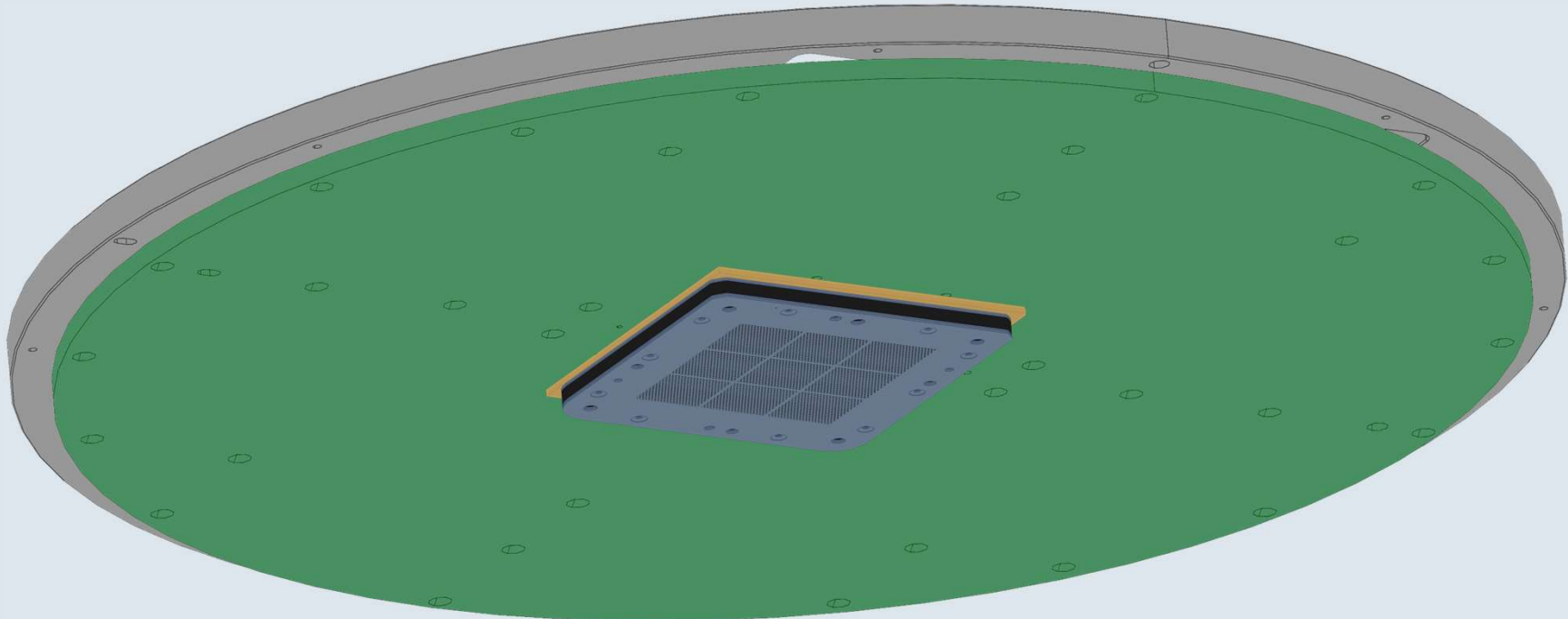


What we do

Technoprobe operates both at wafer-level and in final testing

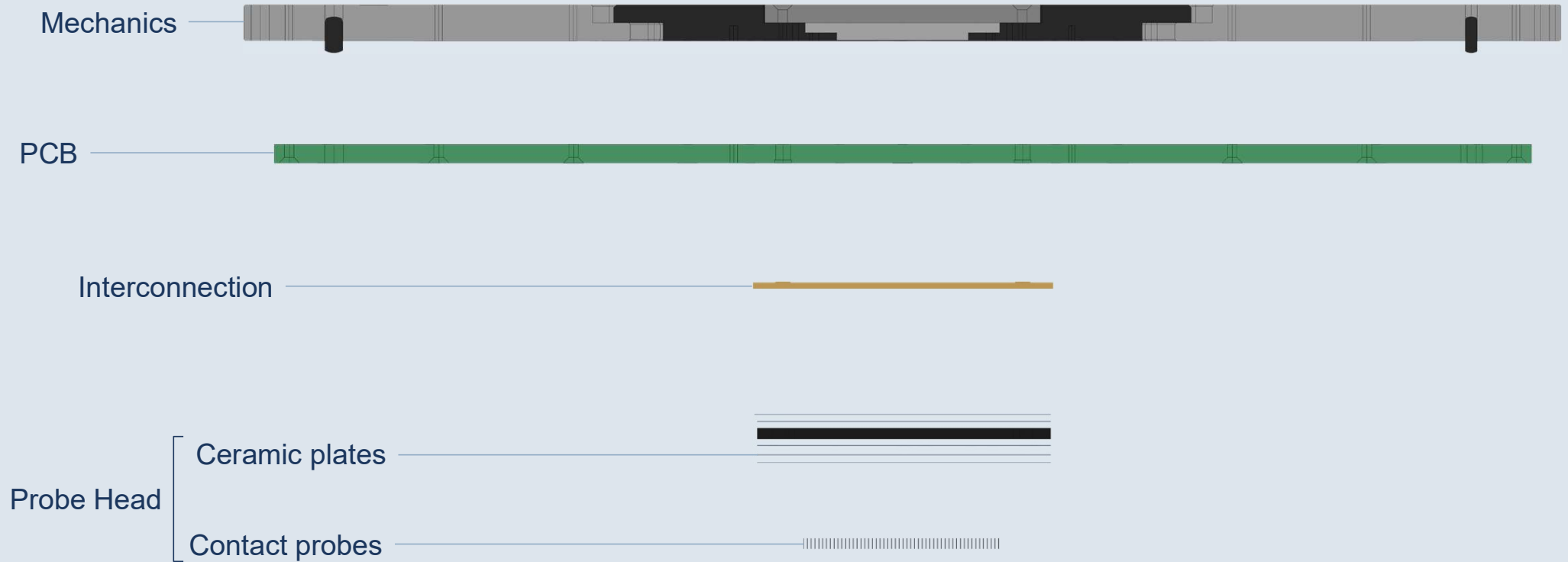


The Probe Card





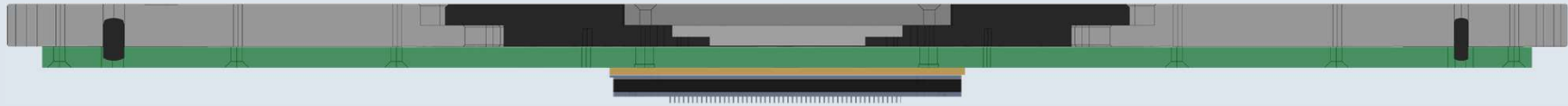
The Probe Card





The Probe Card

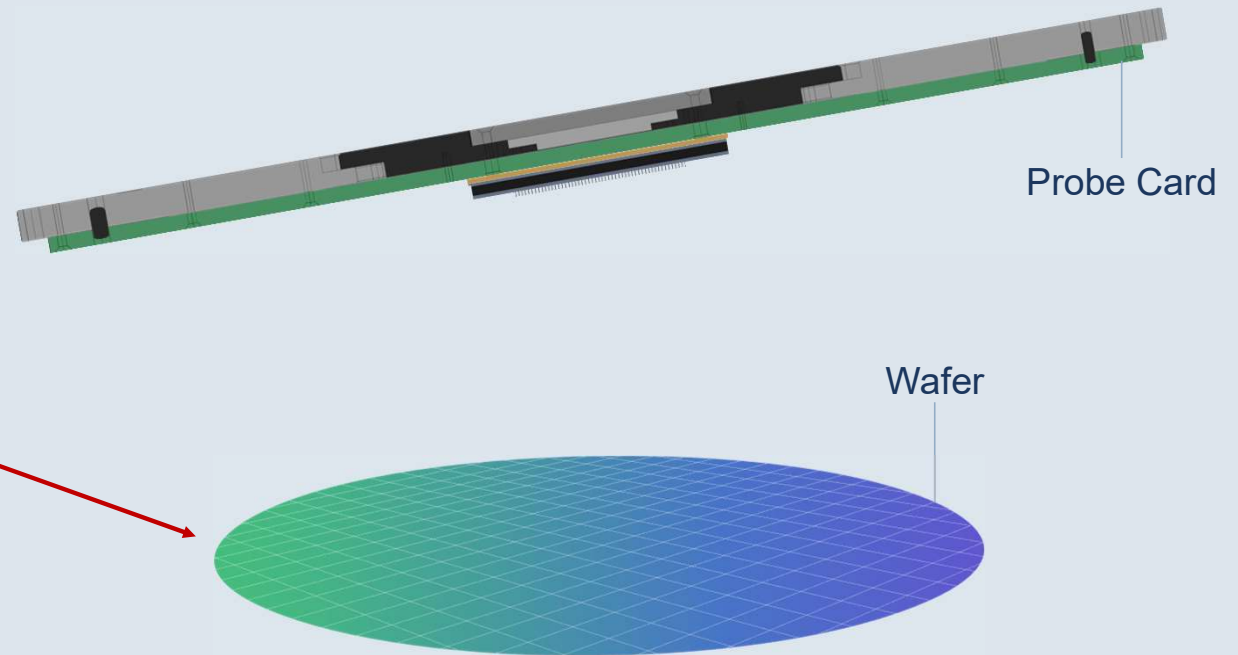
The Probe Card has very thin needles (**probes**) that touch the terminals (pads) of chips, thus electrically connecting to a **tester**.





The Probe Card

The Probe Card has very thin needles (**probes**) that touch the terminals (pads) of chips, thus electrically connecting to a **tester**.





Reference Market



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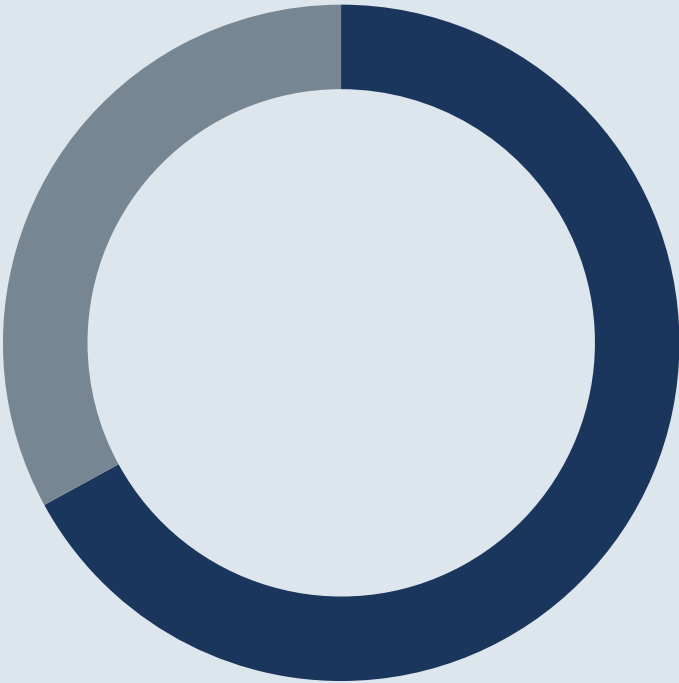
Overview of the Semiconductor Probe Cards market



2024 Semiconductor Probe Cards Market*

Overall market value: \$2.4bn

Memory applications
\$805m



Non memory applications
\$1.638m

*Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.

2024 Non-memory applications market share



TECHNOPROBE

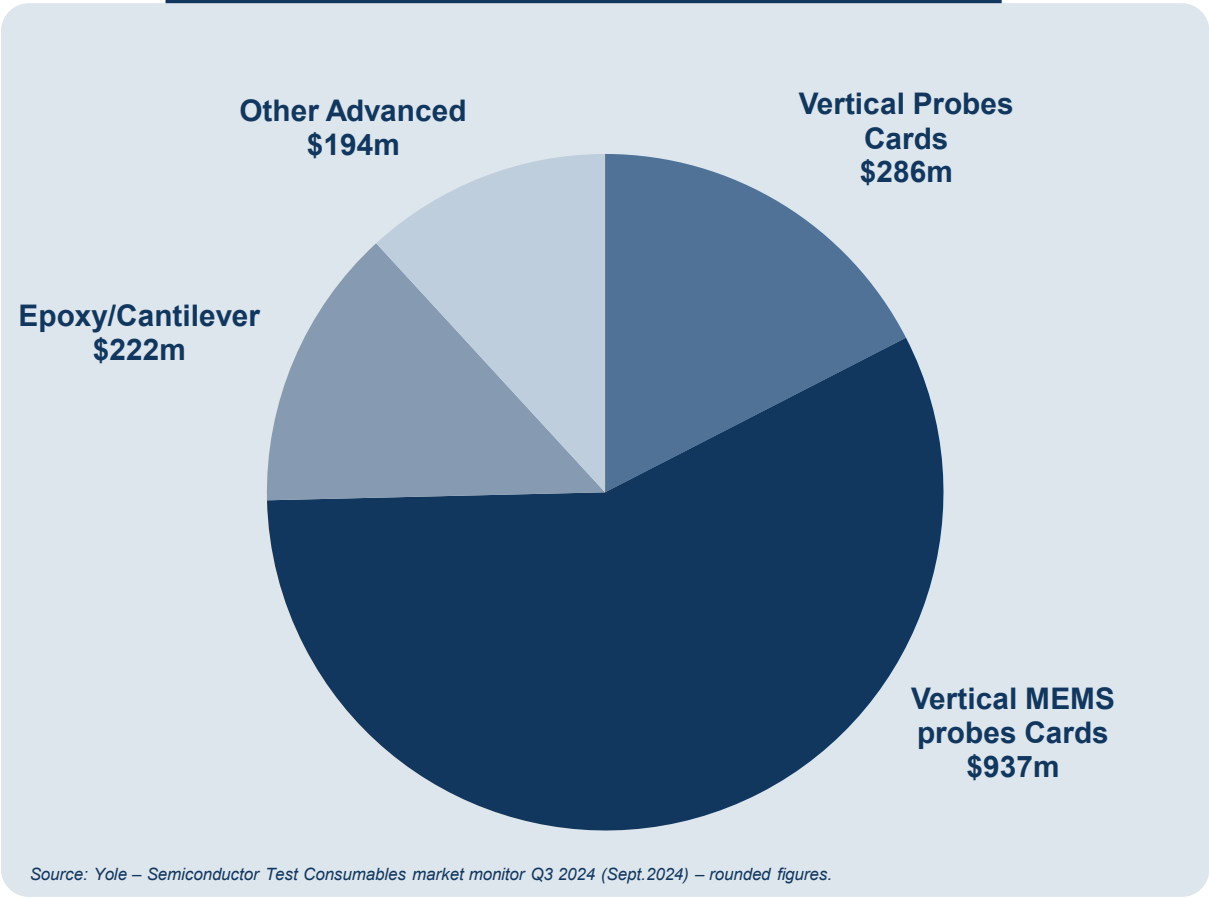


34%

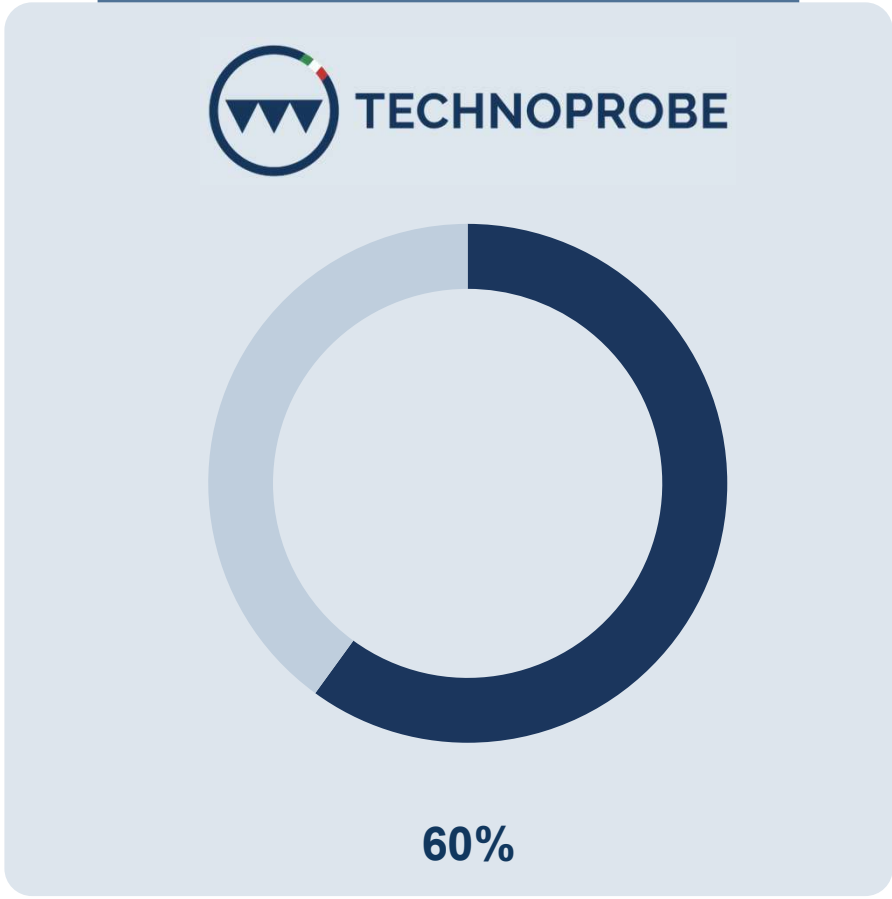
Overview of the Semiconductor Probe Cards market



2024 Non-Memory applications by type*

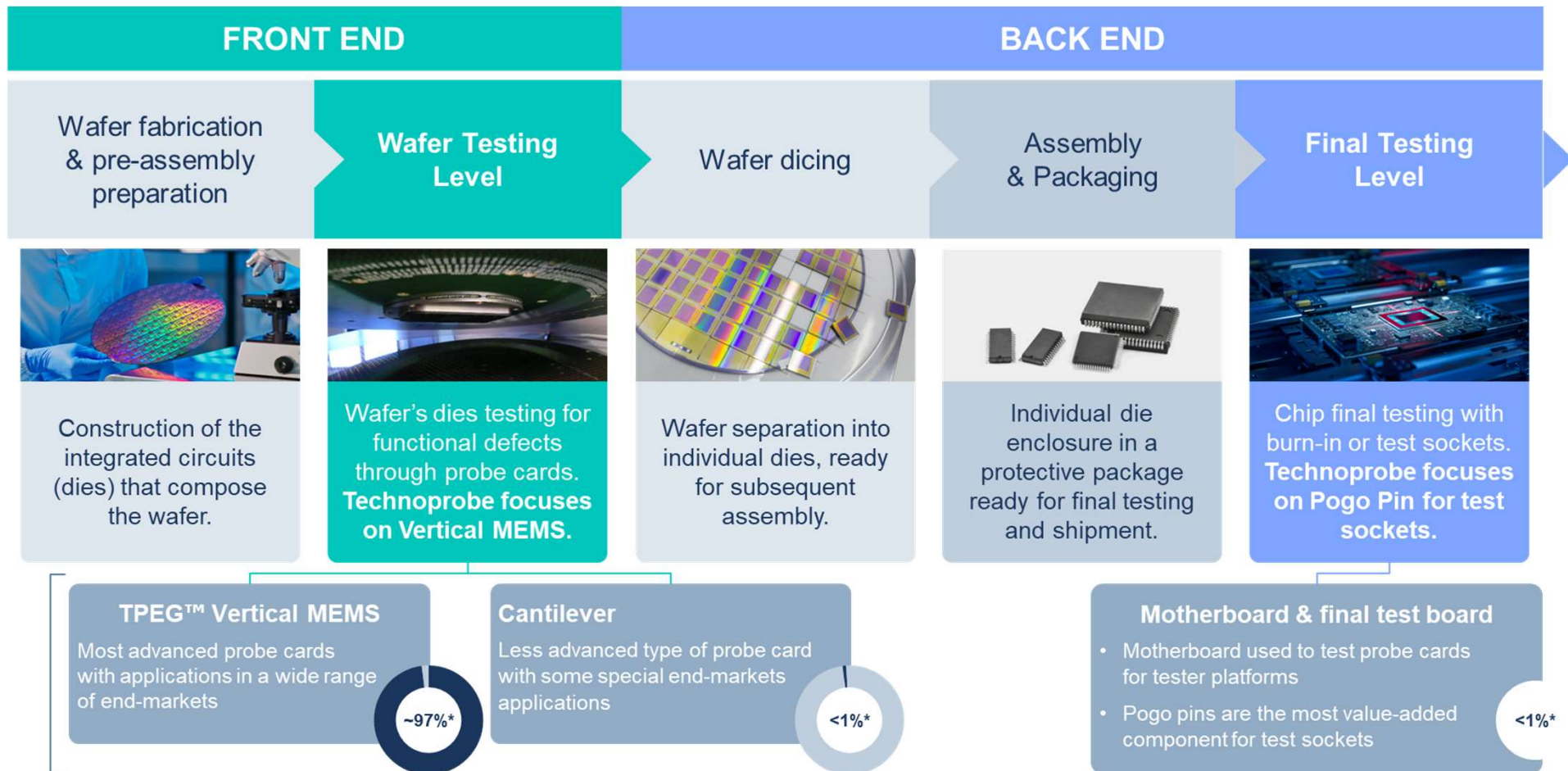


2024 Vertical MEMS Probe Cards market share



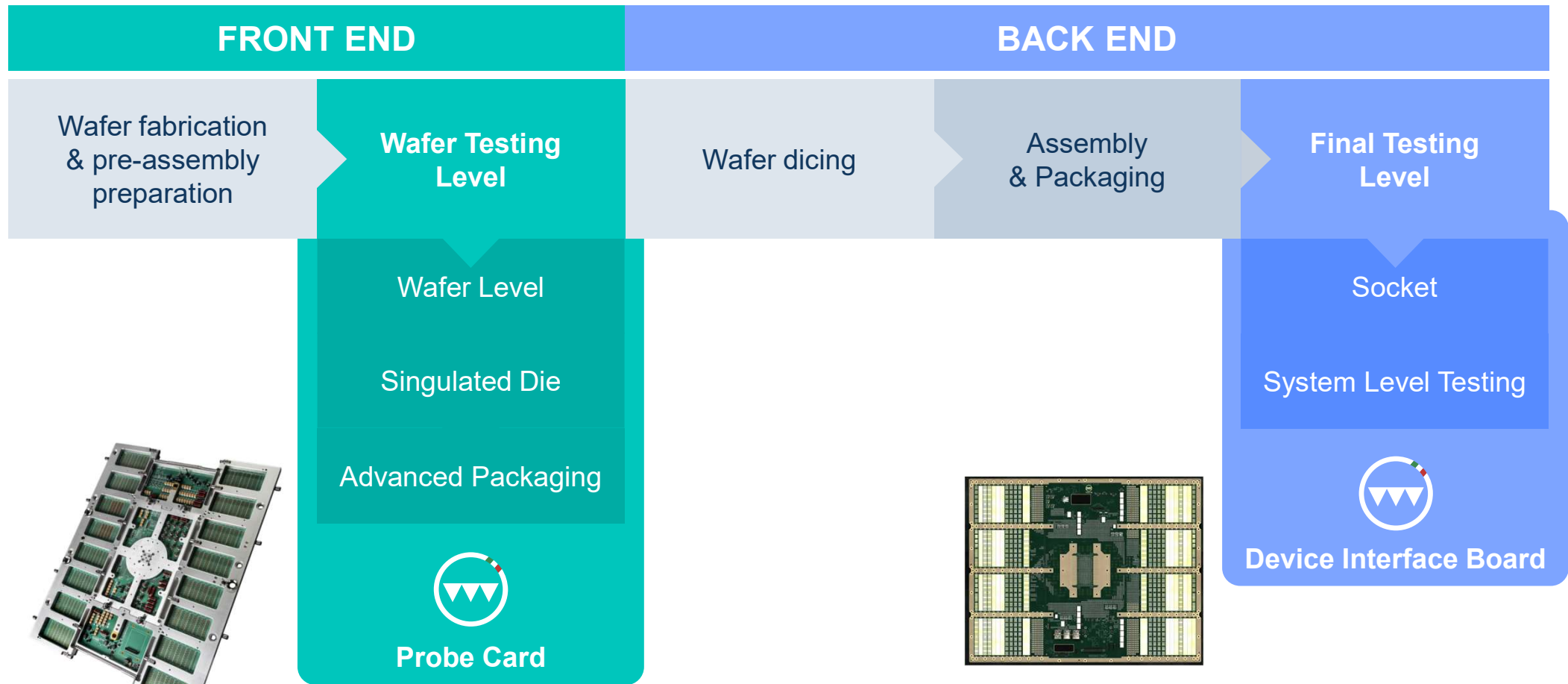


Probe Cards in the semiconductor manufacturing process





Our positioning in the testing space





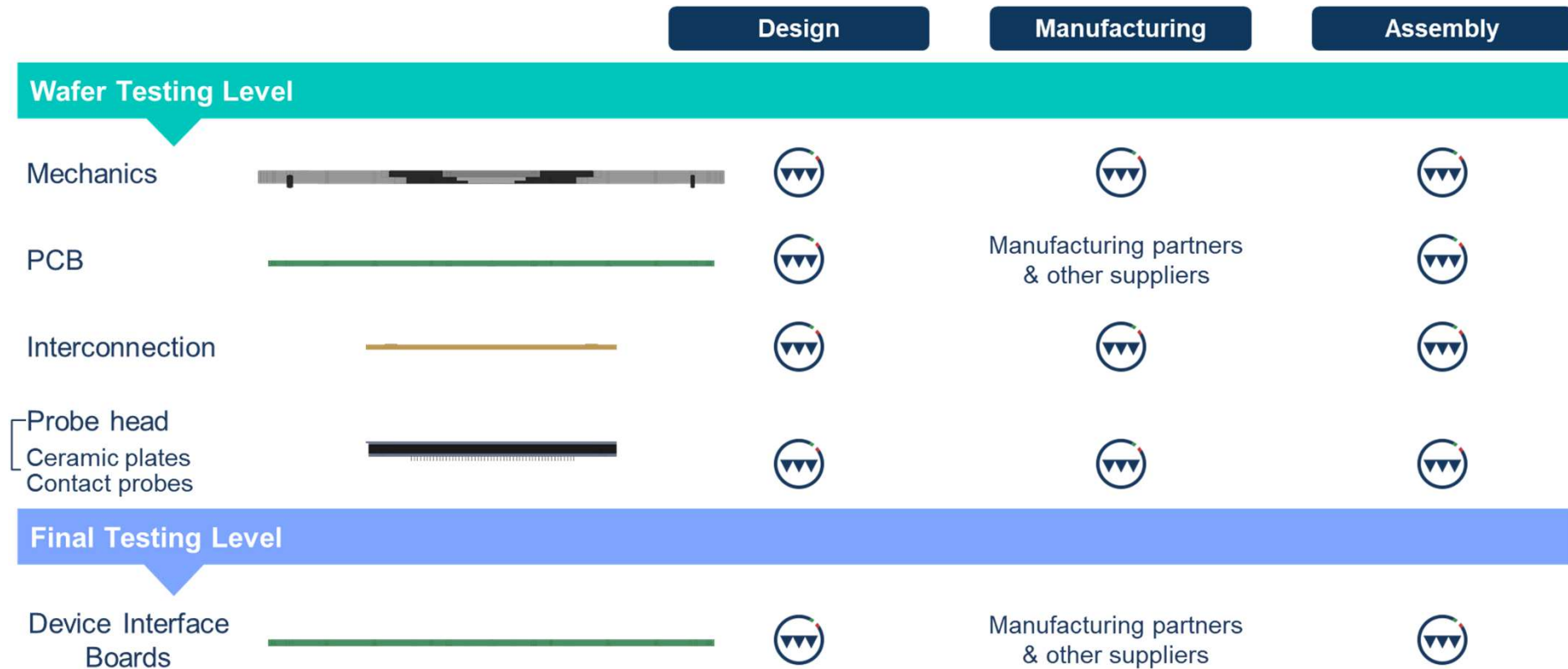
Business Model



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A successful and vertically integrated business model



Built an open eco-system partnerships



TERADYNE

Accelerate growth of
complete Probe Card and
Final Test Interfaces by
acquisition of DIS

Joint Development Projects
to deliver superior customer
value in SOC and Memory



TECHNOPROBE

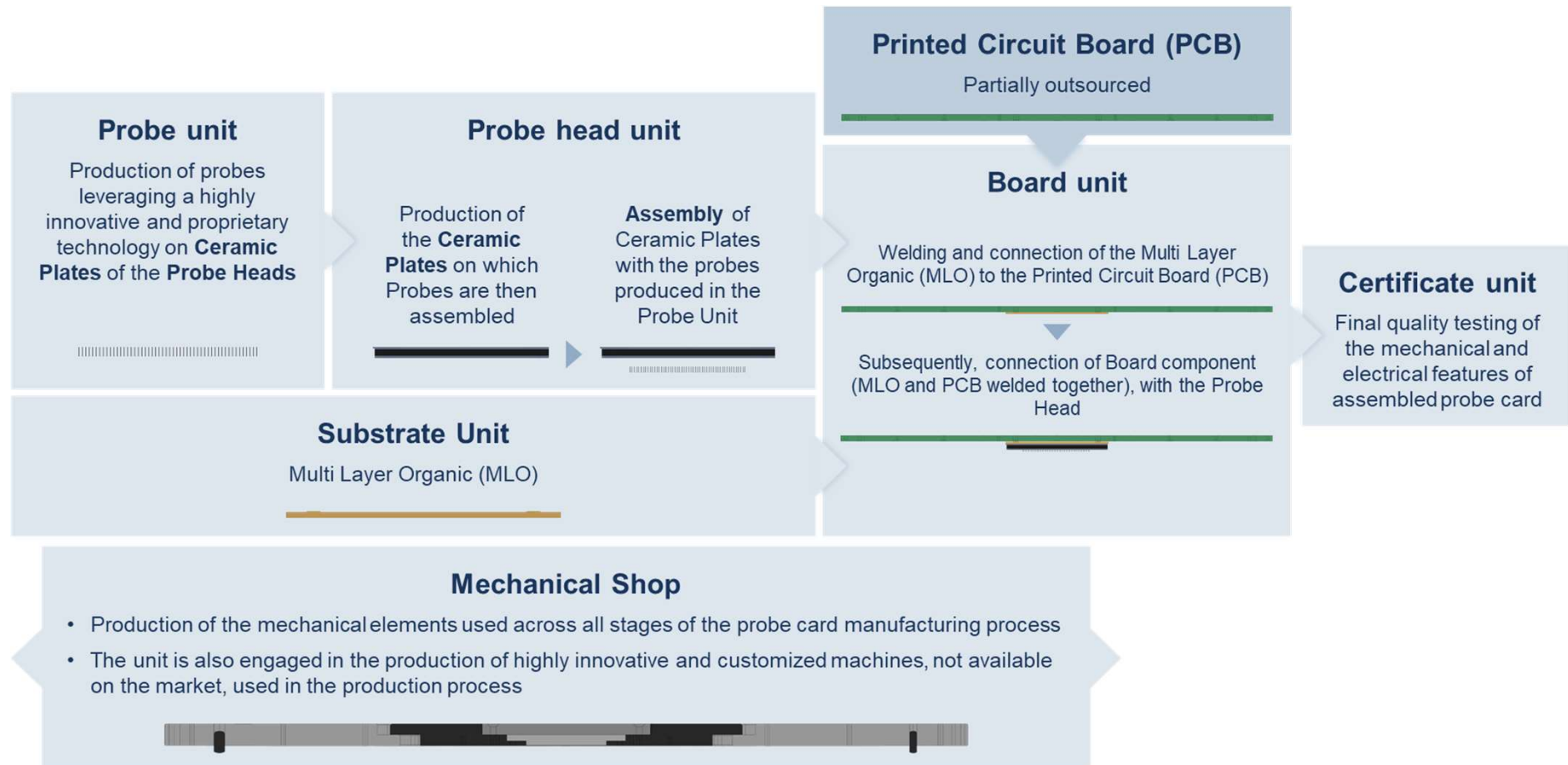
ADVANTEST

Priority suppliers
of PCB

Joint Development Projects
to share knowledge



Overview of the Probe Cards manufacturing process

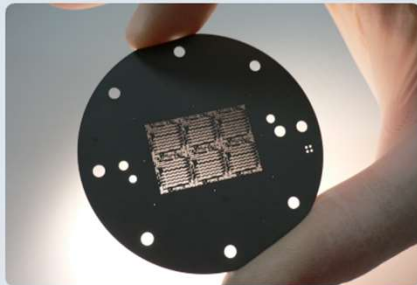




A wide range of highly innovative technologies

Advanced micromachining

Advanced laser cutting:
high accuracy and fast lead time



Thin film

Strong investment in advanced thin film technology to reduce lead time and improve quality and complexity



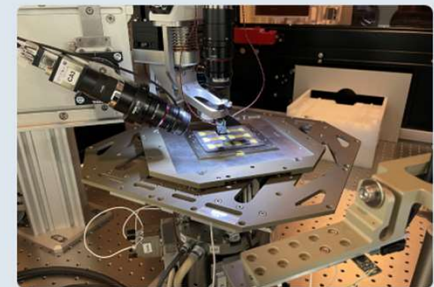
3D MEMS

Acquisition of MICROFABRICA in 2019; the sole company in the world specialized in 3D metallic MEMS manufacturing



Advanced manufacturing

Advanced manufacturing for high volume and best quality assembly of micro components





Vision & Strategy



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Challenges & strategic setting

1

Evolution of chip technology (more than Moore)

Scaling slow down as enabler for **chiplets**,
3D architectures and **new materials**

→ Continuous investments in R&D

→ M&A as accelerator of
technological development

2

Increase in complexity

Design and manufacturing are becoming essential
capabilities to reliably deliver **complex solutions**

→ Strategic partnerships

→ Vertical integration of the most value-
added components of the probe card

3

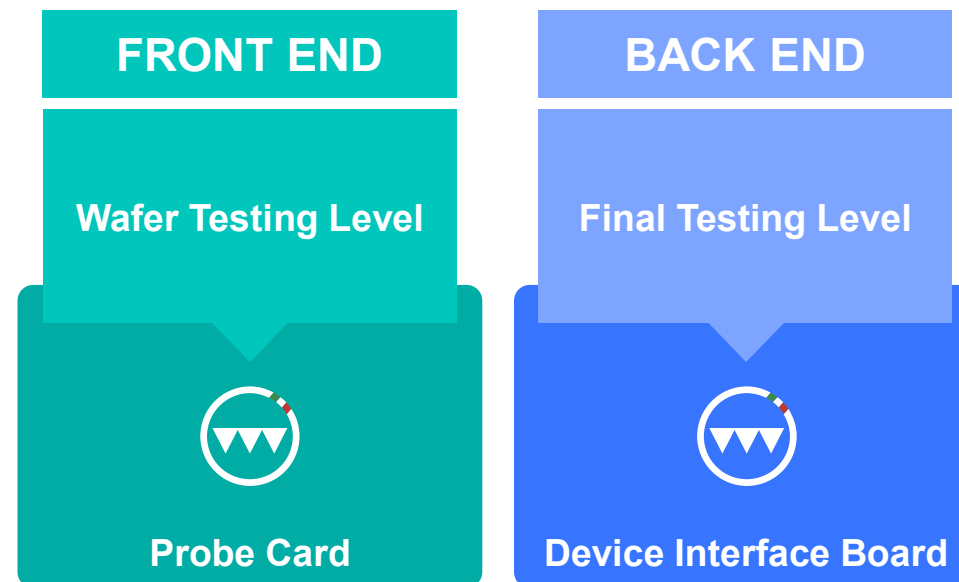
Client satisfaction

Reliability of the product & **on-time delivery**

→ Support on site

→ Commercial agreements

What's next?





What's next?

Consolidate the leading positioning in all test segments

FRONT END

Drive advancements in Logic Semiconductor Testing

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

Enter the High Bandwidth Memory (HBM) segment

BACK END

Strengthen positioning in Final Testing

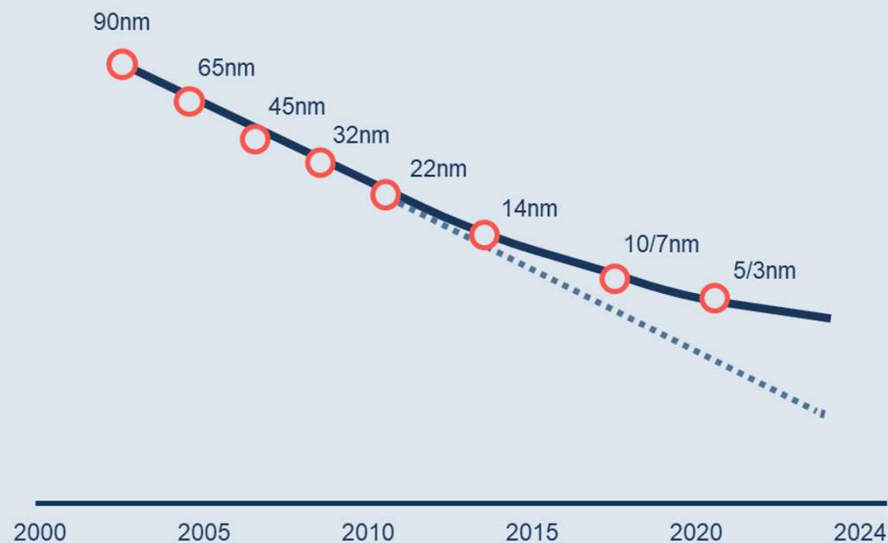


Semiconductor technology trends

Industry motivation behind advanced packaging

How to continue drive for increase compute power in light of transistor density rate lower and die size growth limitations?

Transistor scaling rate is decreasing



Die size scaling limited by reticle size and yield optimization





Semiconductor technology trends

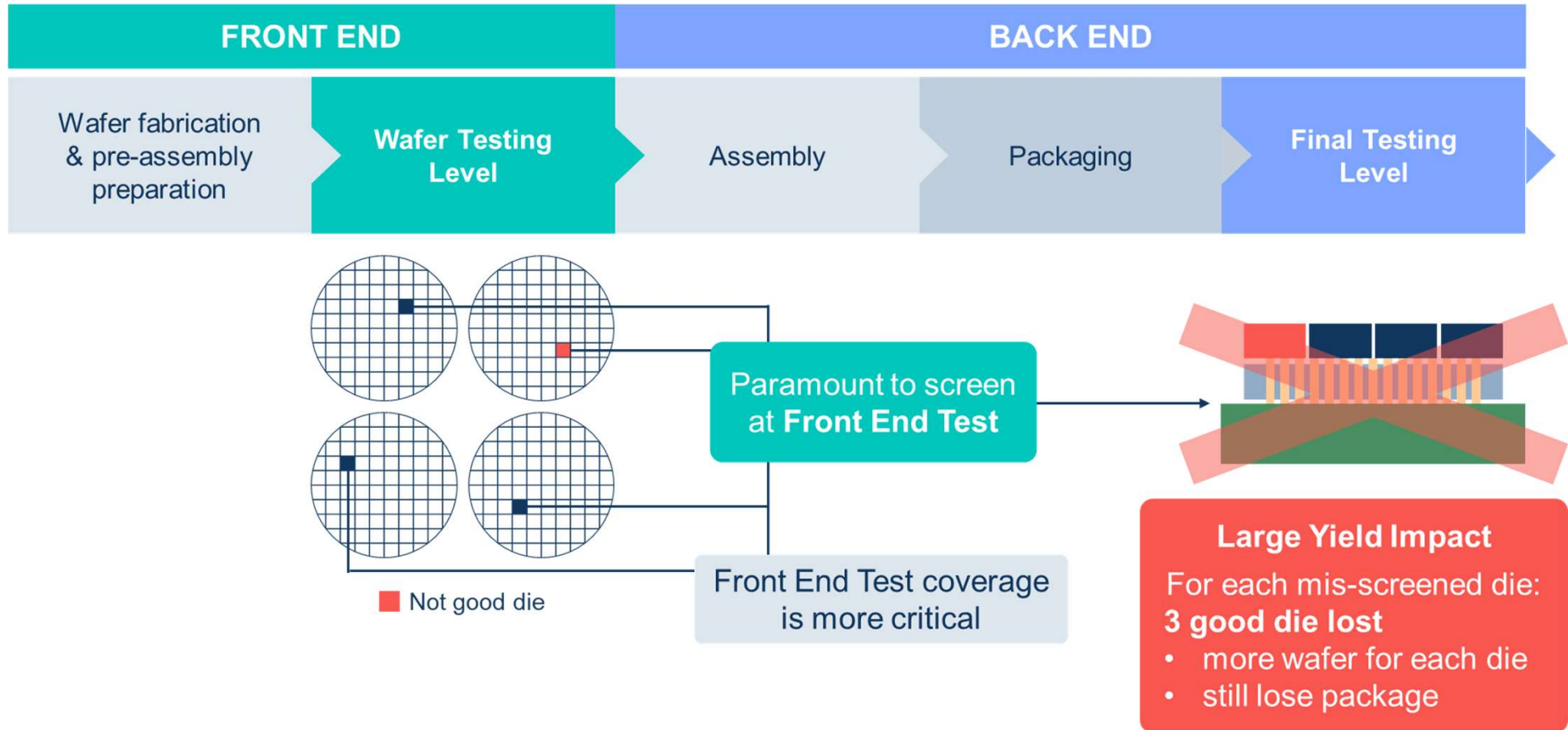
Solution: die disaggregation and advanced packaging



- Improved wafer-level yield with smaller chiplet
- Optimizing performance with mixed functionality capabilities
 - Memory
 - Co-packaged optics
- Allows for mixed technology node application and IP reuse

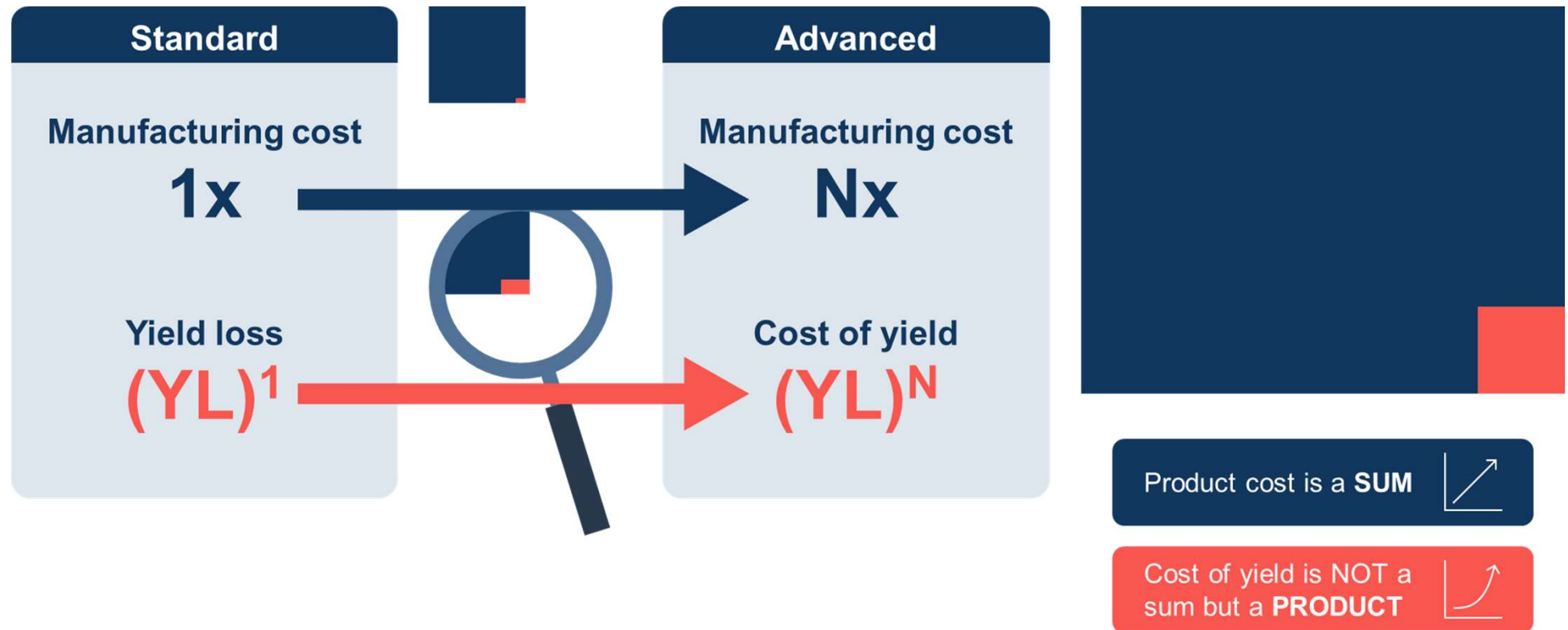


Semiconductor technology trends





Advanced packaging versus standard





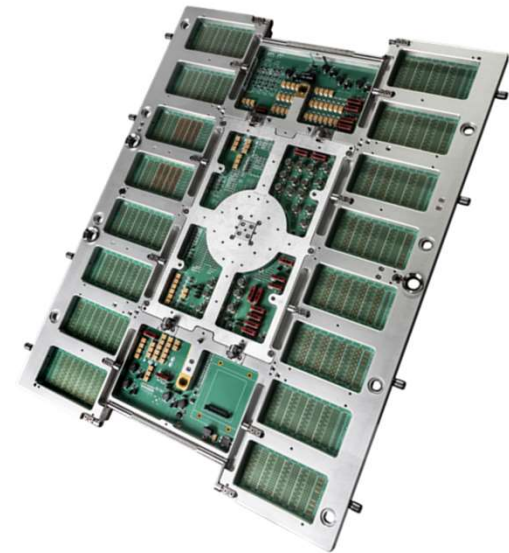
Advanced packaging versus standard



Front End Test coverage
is more critical

True **Known Good Die** required!

SOLUTION
more test at probe
=
more **Probe Cards**





Technoprobe as advanced packaging enabler

Fine pitch and ultra-large pin count

Necessary to effectively probe HPC and HBM's and all leading-edge product

High-speed

Short, ultra short and RF-specific needles technology to manage high speed interconnect IO, including SiPh

High power and thermal

Delivering high power to DUT in effective and reliable way

Ability to remove heat dissipated by the probe card (directly or because of power transferred from DUT to PC)

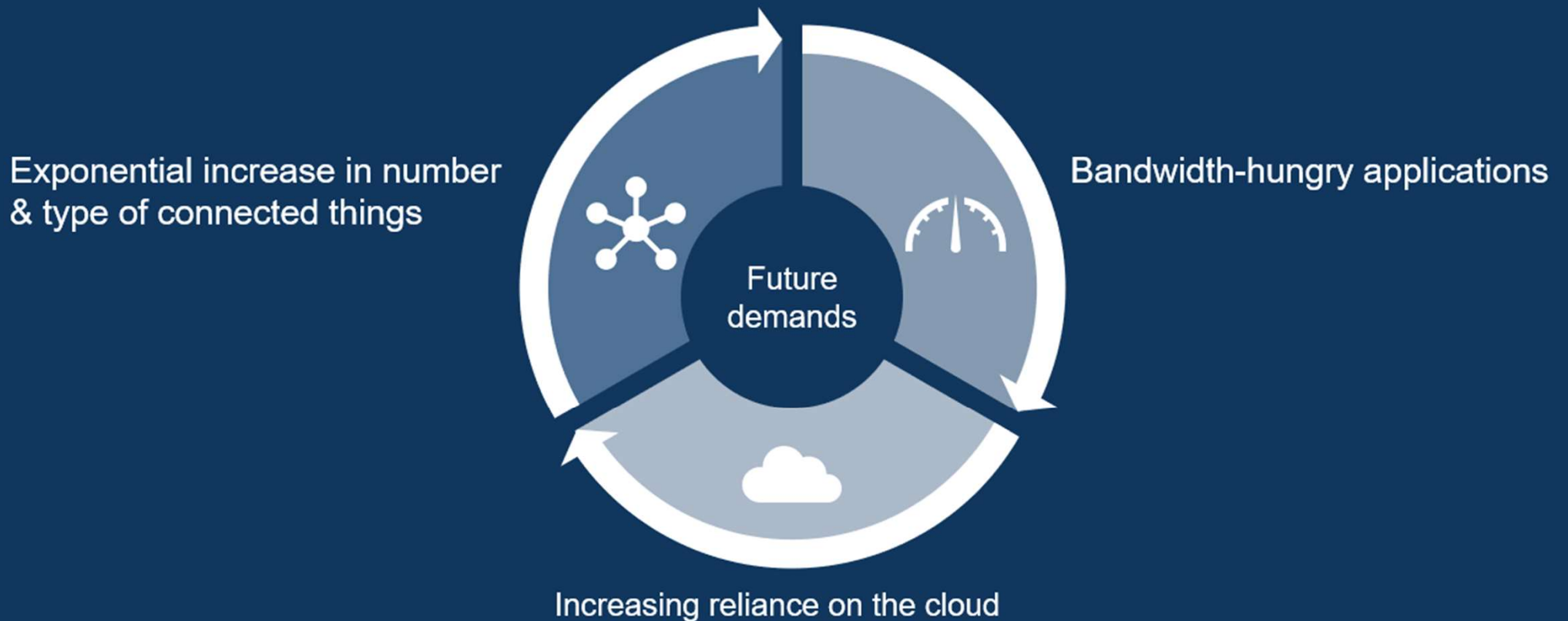
High-density interconnect

Ultra-high complexity PCB and MLO/MLC for resource fan-out on ATE/SLT



A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:



FRONT END Proliferate high-speed, high-voltage, radio frequency and silicon photonics

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A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Proliferation of connections

Analog radio frequency

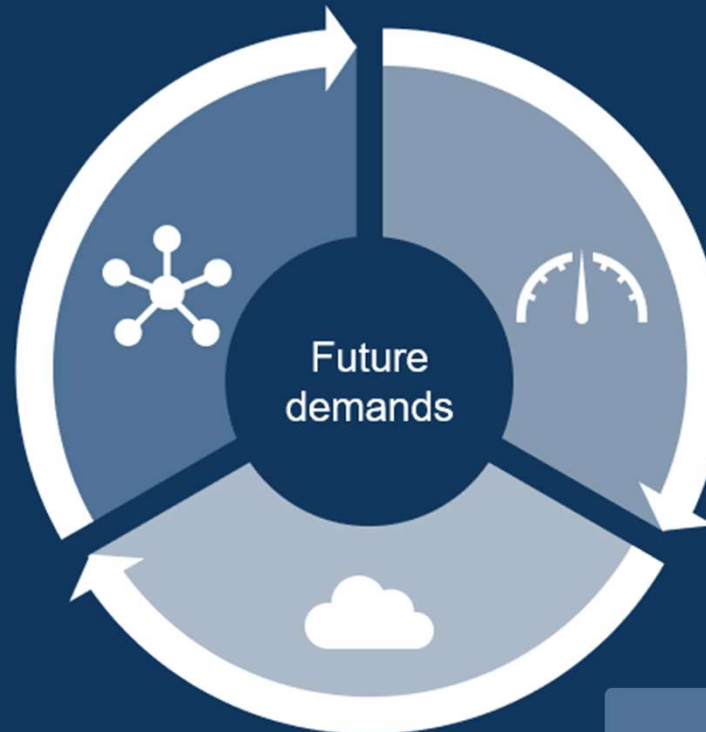
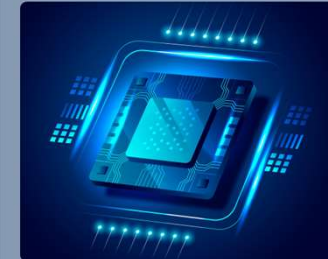
Satellite communications and sensing, automotive radar, mobile communication,...



Bandwidth - hungry applications

Silicon photonics

Chiplet to chiplet interconnect / photonics-driven computing



Increasing reliance on the cloud

Chiplet probing

High density and high-speed IO inside chiplet demand for high-performance probe needles

FRONT END Proliferate high-speed, high-voltage, radio frequency and silicon photonics

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A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Silicon photonics

Technoprobe technologies integrated in the same product enable...

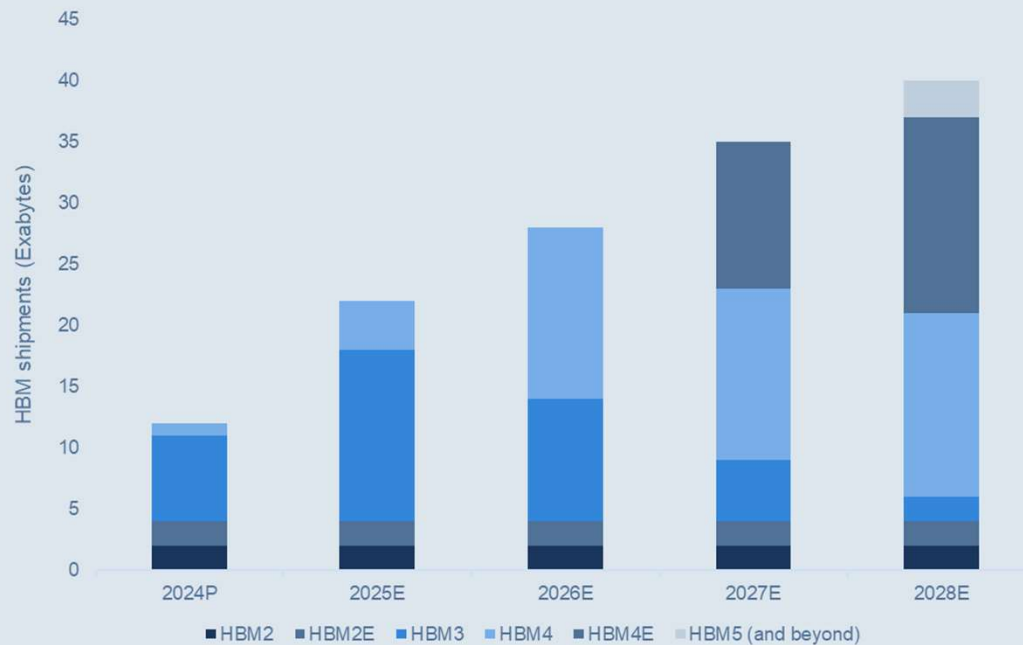
- | | |
|---|--|
| Fine pitch probing | → alignment with advanced packaging roadmap |
| Radio frequency probes | → high-speed performances in same probe card solutions |
| Technoprobe IP | → usage of standard wafer prober |
| Integration of other IP from specific segment suppliers | → flexibility and compliancy with customer preferred test method |

FRONT END Proliferate high-speed, high-voltage, radio frequency and silicon photonics

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DRAM & HBM: complexity as driver to new products



Source: Yole DRAM market monitor Q1 2025.

- HBM demand continues to grow
- HBM bandwidth requirements almost double gen-gen

FRONT END Enter the High Bandwidth Memory (HBM) segment

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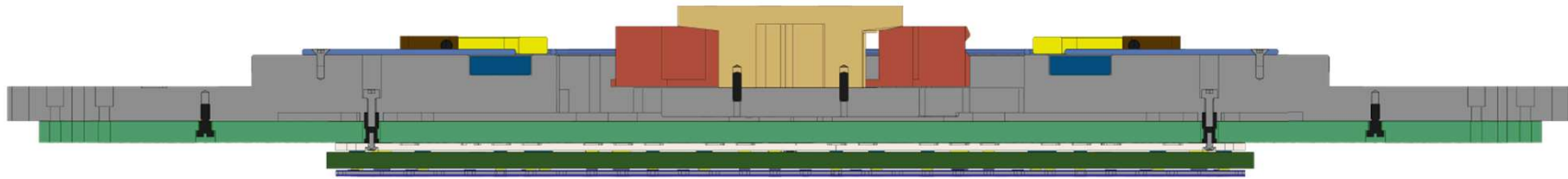


DRAM & HBM: complexity as driver to new products

DRAM and HBM are typically tested with **microcantilever** probing technologies.

Most **advanced HBM** and Next Generation products are becoming more challenging in terms of pad pitch, signal integrity, and power.

For both applications Technoprobe is leveraging on **Vertical MEMS** solution and on a unique PC architecture.

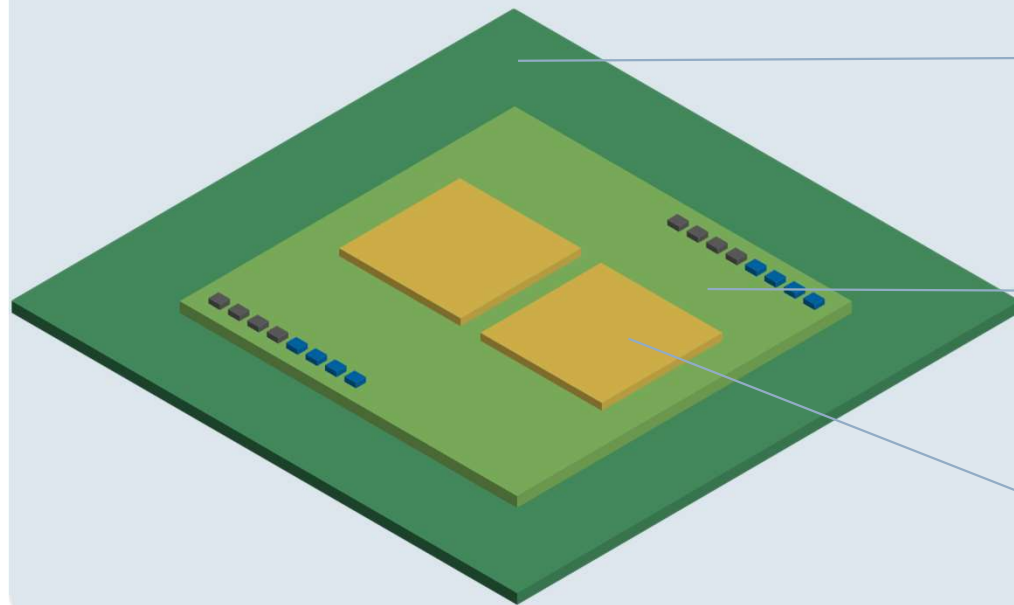


FRONT END Enter the High Bandwidth Memory (HBM) segment

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FUSIONLINK

We have applied the disaggregation to test interface hardware



Main motherboard

Best technology: printed circuit board (PCB)

Device substrate

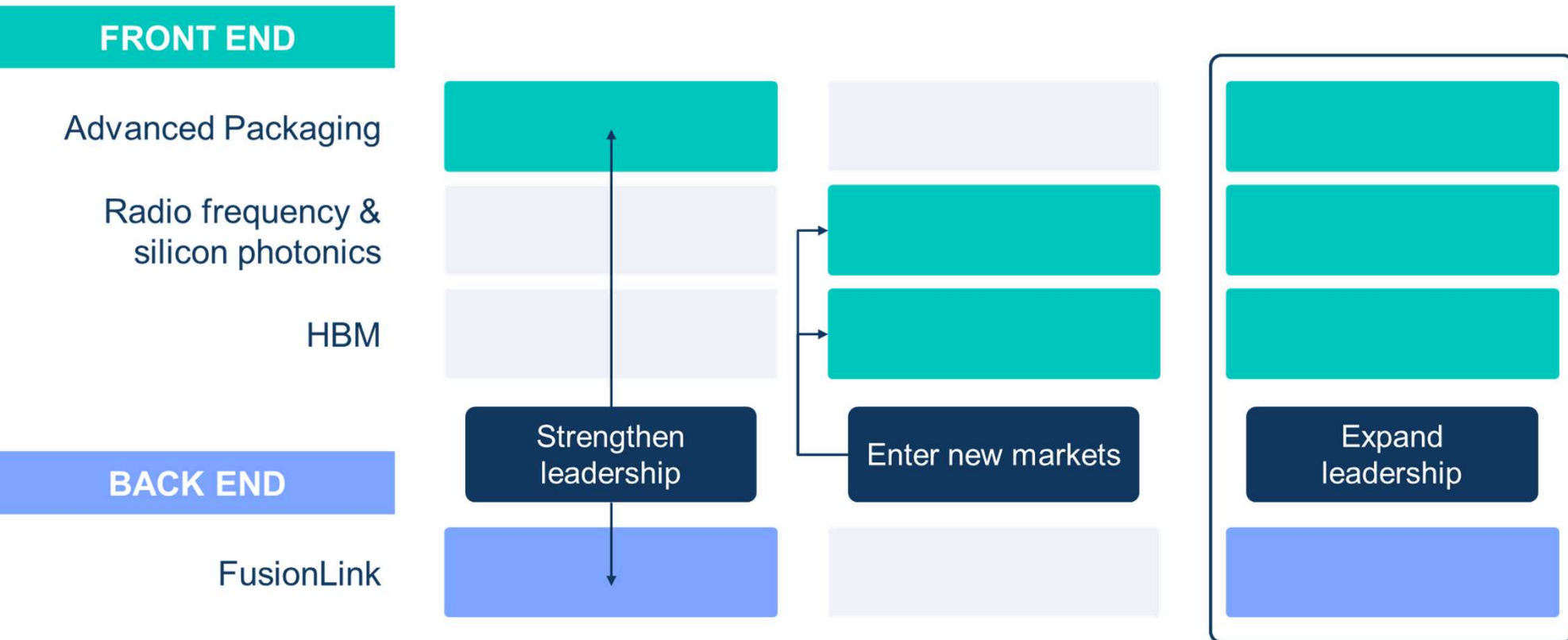
Best technology: high density interconnect (HDI)

Probe substrate

Best technology: multi-layer organic (MLO)



Growth drivers & trajectories





Financial Outlook



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Mid-terms scenario

1 Technological complexity evolution

- Testing solution for Advanced Packaging
- Increase in demand for high-precision tests

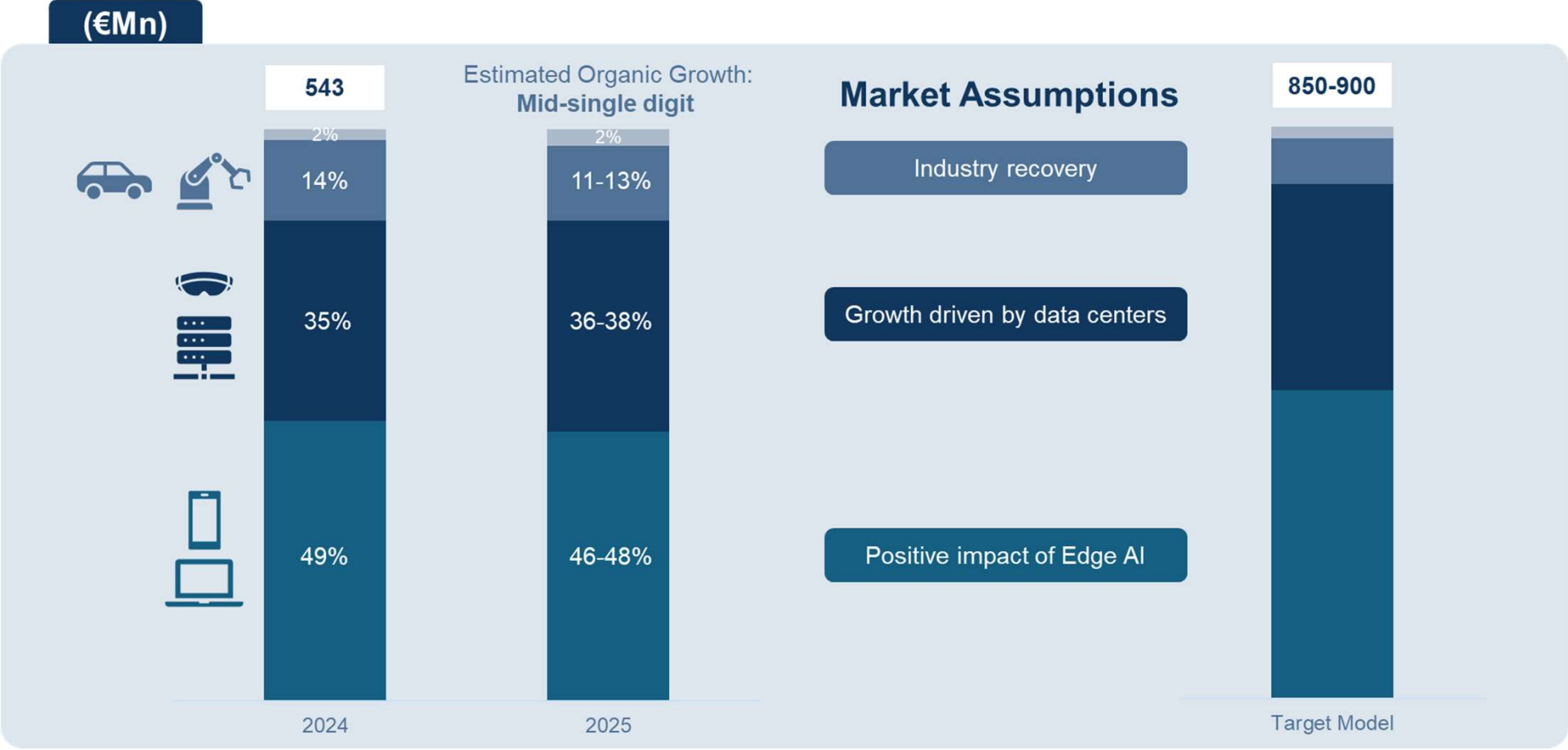
2 Market trends

- AI will lead the growth for many market segments
- Expansion of memory semiconductor segments

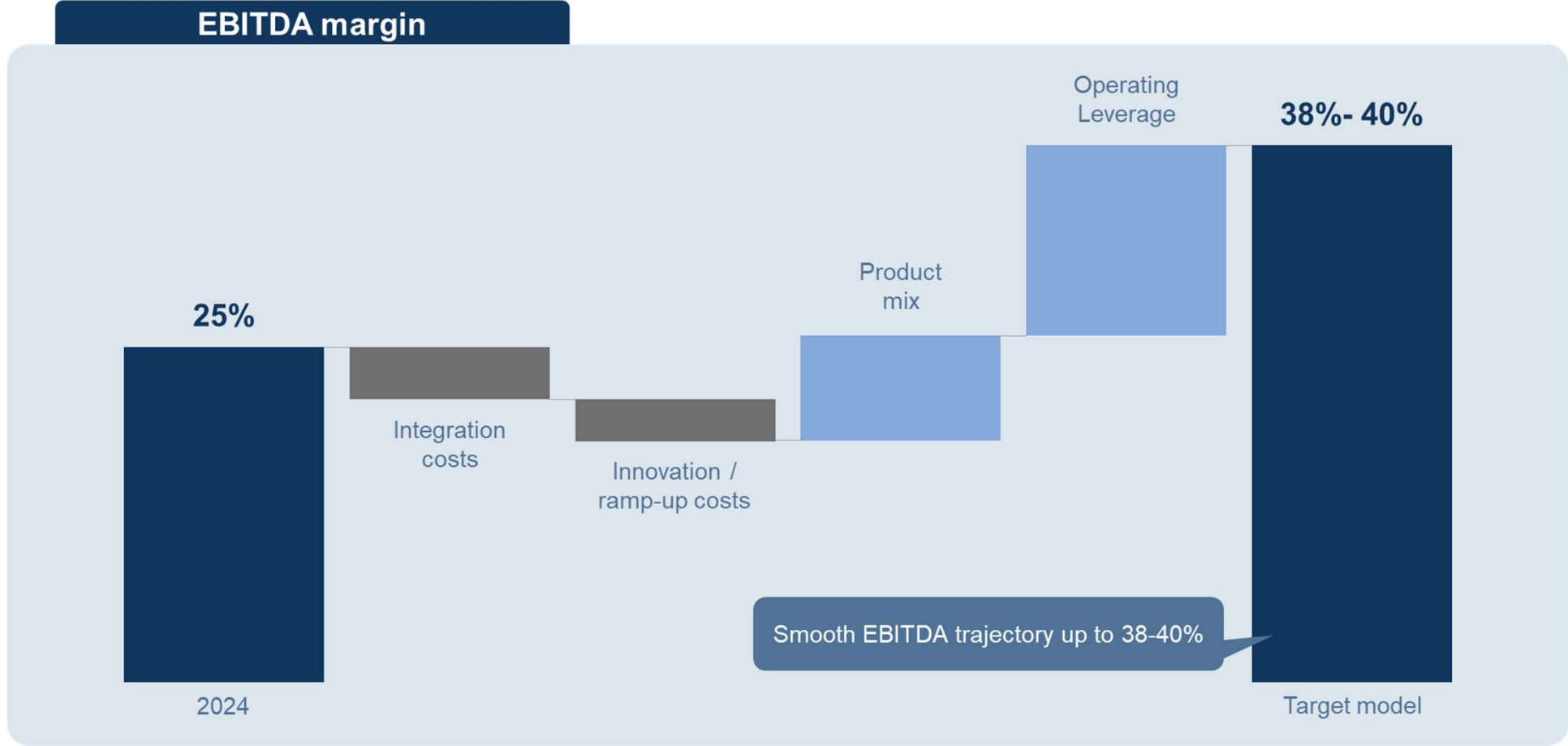
3 Geo-political instability

- Technological sovereignty
- Commercial policies

Market trends & revenues path



Profitability profile

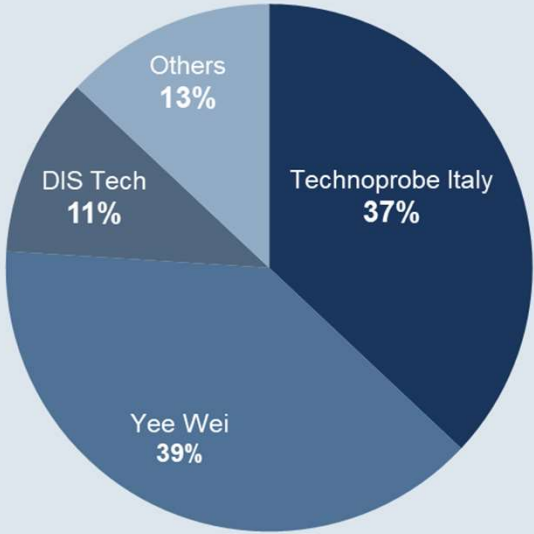


Capex



(€Mn)

FY 2024



	FY 2022	FY 2023	FY 2024	Target Model
Revenues	549	409	543	
Capex	84	73	100	
Capex as % of Revenues	15%	18%	18%	8% - 10%



H1 2025 Results



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H1 2025 Market Drivers

Revenues at 325.9€m

up 7.3% QoQ
up 35.2% YoY



Consistent growth in AI



Slight increase in Consumer market



Weakness in Automotive only partially offset by upward trend in Industrial





Financial Highlights

Q2 2025

Revenues were **168.7€m**

up 21.1% YoY, up 7.3% QoQ

Gross Profit was **79.9€m**

up 38.4% YoY, with a margin of 47.3%

Ebitda was **58.3€m**

up 61.8% YoY, with a margin of 34.6%

H1 2025

Revenues were **325.9€m**

up 35.2% YoY

Gross Profit was **150.6€m**

up 49.5% YoY, with a margin of 46.2%

Ebitda was **106.4€m**

up 75.2% YoY, with a margin of 32.6%



Financial Highlights

	H1 2025	H1 2024	YoY Variance	Comments
€m				
Revenues	325.9	241.1	+35.2%	• Benefit from: ○ Organic growth: rising trend in AI and slight increase in consumer, partially offset by shrinkage in auto and industrial ○ Change of perimeter (6 months of DIS revenue in H1'25 vs 1 month in H1'24)
Gross profit	150.6	100.8	+49.5%	• Gross profit margin benefitted from: ○ Recovered production efficiency ○ Operating leverage effect
% margin	46.2%	41.8%		
EBITDA	106.4	60.7	+75.2%	• Ebitda margin, in addition to the above, benefitted also from US reorganization positive impact
% margin	32.6%	25.2%		
	30.06.2025	31.12.2024		
Net Financial Position	641.9	656.3		• Net financial position: variance mainly attributable to solid cash flow from operating activities (+69€m), offset by capex (-28€m), the acquisition of a minority stake in Yee Wei Inc. (-20€m) and Innostar Service Inc. (-7€m), together with the unrealized fx impact on foreign currency bank accounts (-29€m).



Q3 2025 Guidance

Revenues: 137€m

(+/-3%)

Gross Margin: 41.2%

(+/-2%)

Ebitda Margin: 28.2%

(+/-2%)



EUR/USD - Accumulated Average by Quarter



Average	Q1 '25	Q2 '25	Q3 '25*	Q4 '25*
	1,052	1,134	1,168	1,186
3M	1,052			
6M	1,093			
9M*	1,119			
12M*	1,136			

* Estimate

Average	Q1 '24	Q2 '24	Q3 '24	Q4 '24
	1,086	1,077	1,098	1,068
3M	1,086			
6M	1,081			
9M	1,087			
12M	1,082			