dbAccess European TMT Conference
Technoprobe S.p.A.

Sept. 4, 2025

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Innovation begins with us

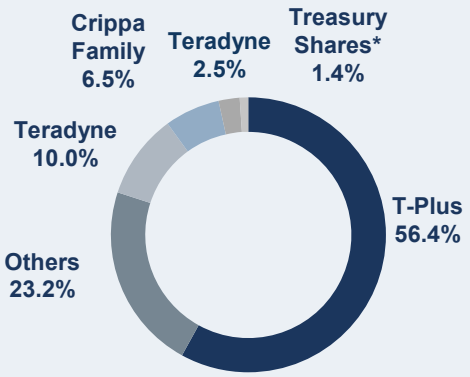
A leading company in the field of semiconductors and microelectronics

Company Overview

2024 Key financial metrics

Revenue	Ebitda	Net Income	Net Financial Position	Mkt Cap
€543.2m **+22%** CAGR 19-24	**€136.5m** **25%** EBITDA margin	**€62.8m** **12%** on revenues	**€656.3m** as at 31/12/2024	**~€4,4bln** as at 1/9/2025

Shareholding Structure



*as at August 29, 2025.

- Leading player in designing and manufacturing of **probe cards**
- Manufacturing process **vertical integrated**
- Strong focus on **innovation**
- Extensive **global presence** and widespread **local footprint**

Where we are

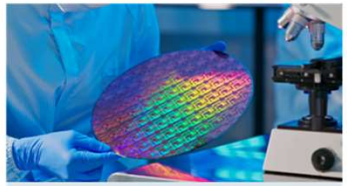
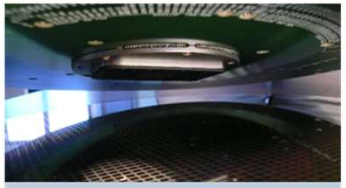
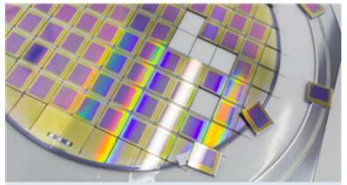
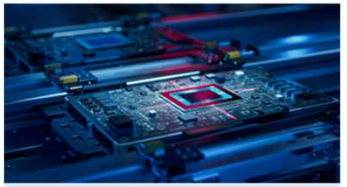
3 Continents

10 Countries

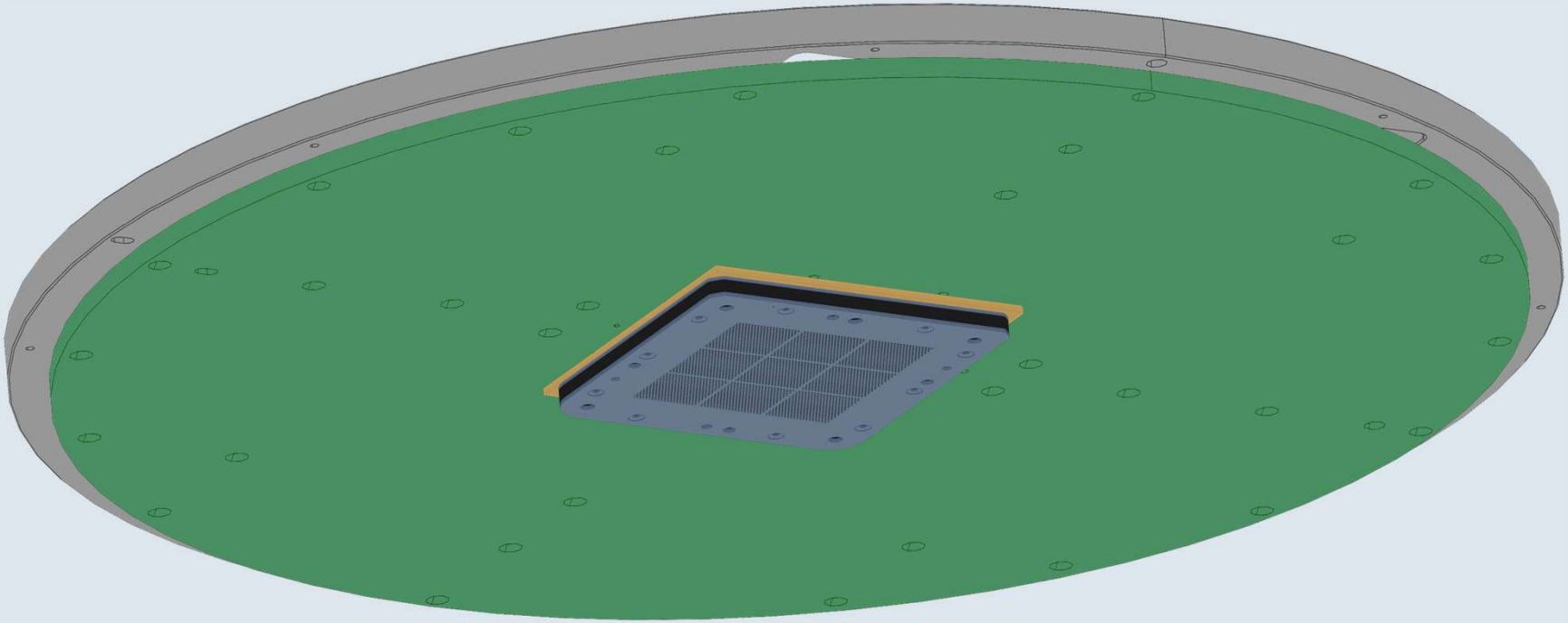
23 Legal entities

What we do

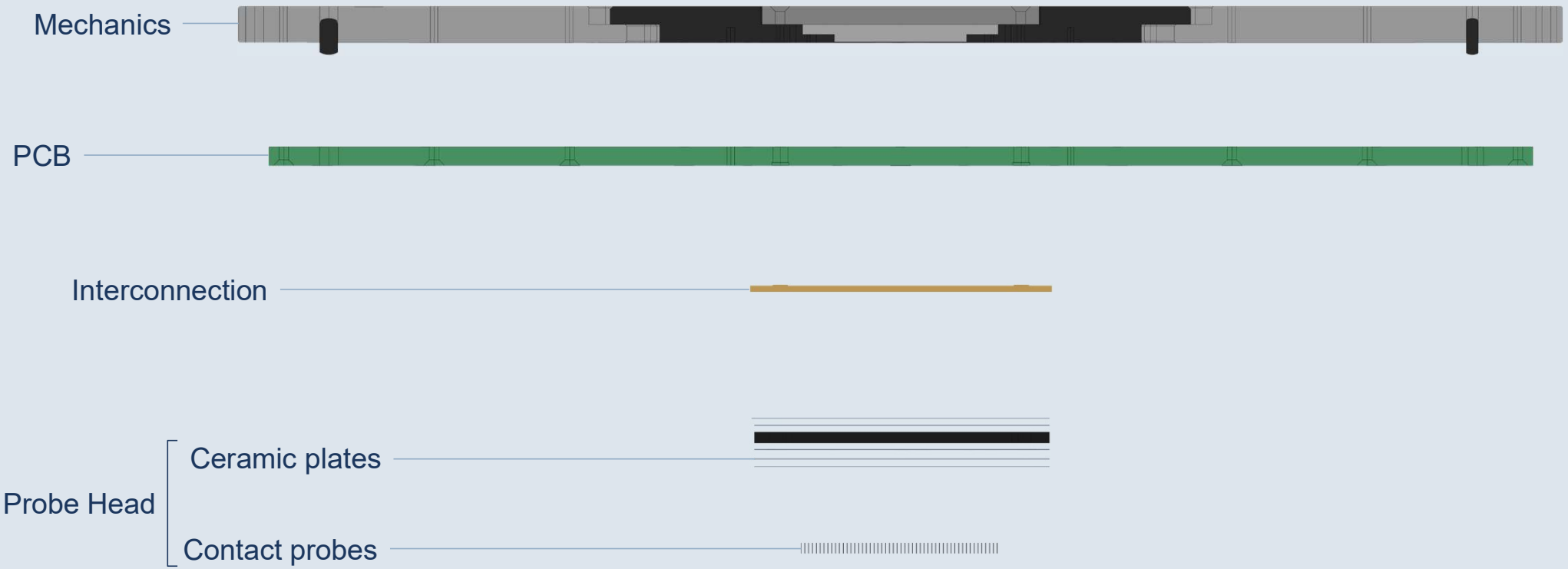
Technoprobe operates both at wafer-level and in final testing

Wafer (multi-chip)	Electrical Wafer Sorting (EWS)	Chip is singulated	Chip is packaged	Final Testing	Integration into electronic devices
Probe Card				Device Interface Board	
					
The silicon wafer contains hundreds of **unsingulated microchips**	The **probe card** electrically tests each chip on the wafer to **check functionality** and **identify any defects**	The wafer is sliced into individual chips, known as **"dies"**	Each chip is **encapsulated** in a package that enables electrical connections and protects it from damage	Packaged chips undergo **final tests** to ensure proper functionality	The packaged chip is **integrated into electronic devices** via printed circuit boards

The Probe Card

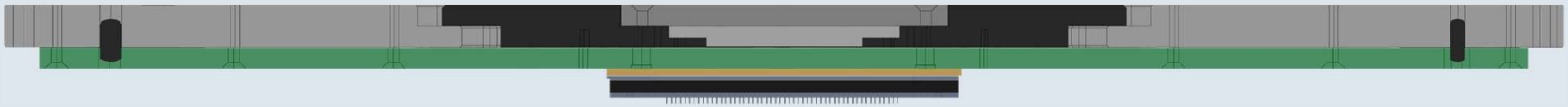


The Probe Card



The Probe Card

The Probe Card has very thin needles (**probes**) that touch the terminals (pads) of chips, thus electrically connecting to a **tester**.



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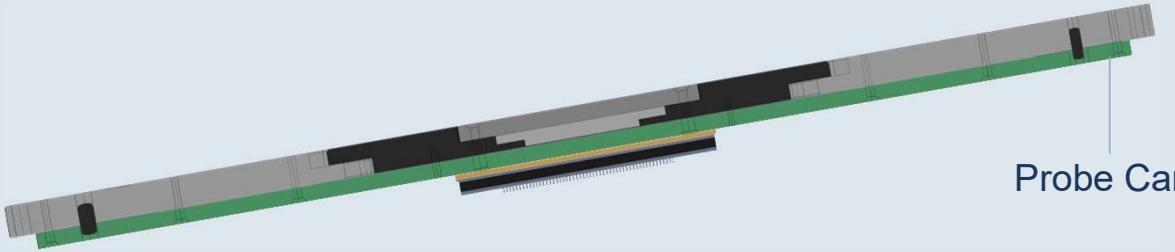
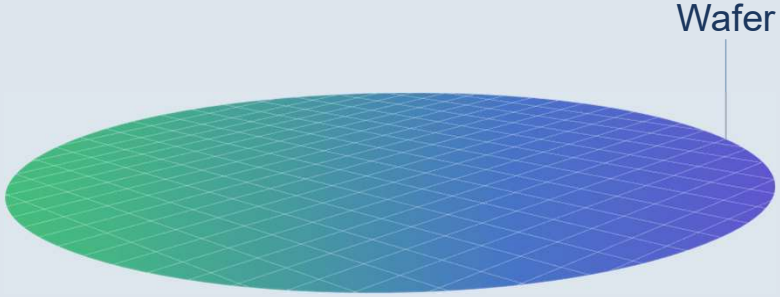


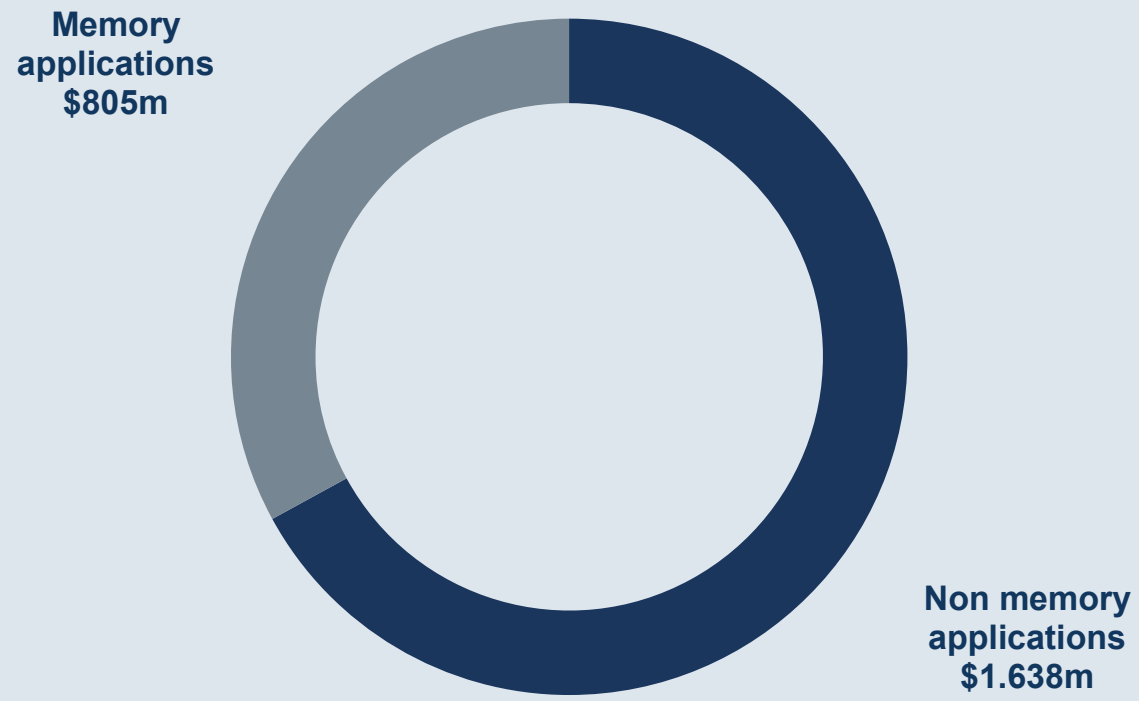


Reference Market

Overview of the Semiconductor Probe Cards market

2024 Semiconductor Probe Cards Market*

Overall market value: $2.4bn



Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.

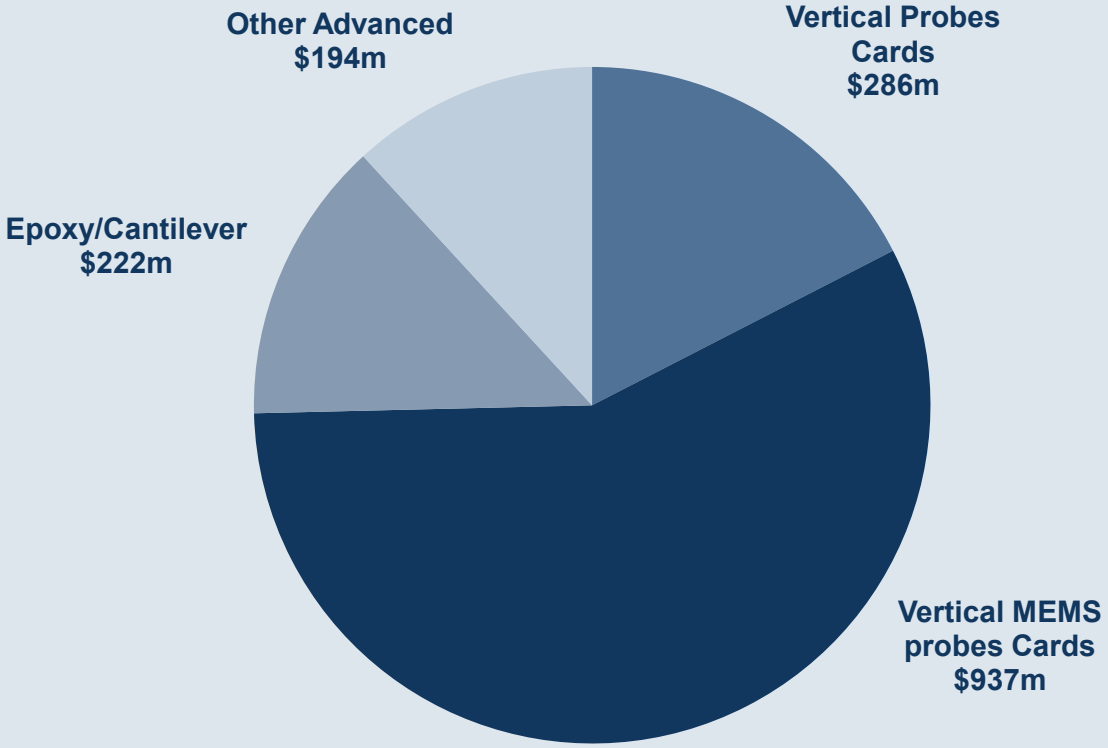
2024 Non-memory applications market share

TECHNOPROBE

34%

Overview of the Semiconductor Probe Cards market

2024 Non-Memory applications by type*



Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.

2024 Vertical MEMS Probe Cards market share

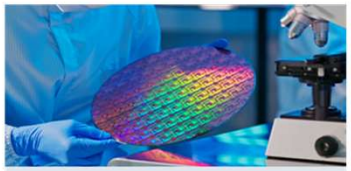
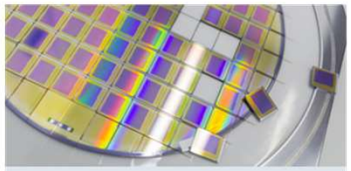
TECHNOPROBE

60%

Probe Cards in the semiconductor manufacturing process

FRONT END

BACK END

Wafer fabrication & pre-assembly preparation	**Wafer Testing Level**	Wafer dicing	Assembly & Packaging	**Final Testing Level**
				
Construction of the integrated circuits (dies) that compose the wafer.	Wafer's dies testing for functional defects through probe cards. **Technoprobe focuses on Vertical MEMS.**	Wafer separation into individual dies, ready for subsequent assembly.	Individual die enclosure in a protective package ready for final testing and shipment.	Chip final testing with burn-in or test sockets. **Technoprobe focuses on Pogo Pin for test sockets.**

TPEG™ Vertical MEMS

Most advanced probe cards with applications in a wide range of end-markets

~97%*

Cantilever

Less advanced type of probe card with some special end-markets applications

<1%*

Motherboard & final test board

- Motherboard used to test probe cards for tester platforms
- Pogo pins are the most value-added component for test sockets

<1%*

Our positioning in the testing space

FRONT END

Wafer fabrication & pre-assembly preparation

Wafer Testing Level

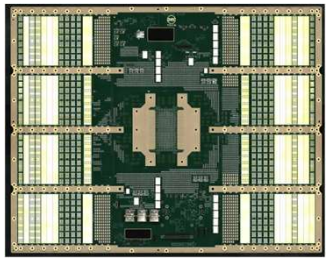
- Wafer Level
- Singulated Die
- Advanced Packaging

Probe Card

Wafer dicing

BACK END

Assembly & Packaging



Final Testing Level

- Socket
- System Level Testing

Device Interface Board

Business Model

A successful and vertically integrated business model

		Design	Manufacturing	Assembly
Wafer Testing Level				
Mechanics		✓	✓	✓
PCB		✓	Manufacturing partners & other suppliers	✓
Interconnection		✓	✓	✓
Probe head Ceramic plates Contact probes		✓	✓	✓
Final Testing Level				
Device Interface Boards		✓	Manufacturing partners & other suppliers	✓

Built an open eco-system partnerships

TERADYNE

Accelerate growth of complete Probe Card and Final Test Interfaces by acquisition of DIS

Joint Development Projects to deliver superior customer value in SOC and Memory

TECHNOPROBE

ADVANTEST

Priority suppliers of PCB

Joint Development Projects to share knowledge

Overview of the Probe Cards manufacturing process

Probe unit

Production of probes leveraging a highly innovative and proprietary technology on **Ceramic Plates** of the **Probe Heads**

Probe head unit

Production of the **Ceramic Plates** on which Probes are then assembled

Assembly of Ceramic Plates with the probes produced in the Probe Unit

Printed Circuit Board (PCB)

Partially outsourced

Board unit

Welding and connection of the Multi Layer Organic (MLO) to the Printed Circuit Board (PCB)

Subsequently, connection of Board component (MLO and PCB welded together), with the Probe Head

Certificate unit

Final quality testing of the mechanical and electrical features of assembled probe card

Substrate Unit

Multi Layer Organic (MLO)

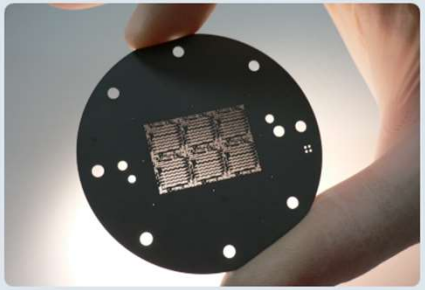
Mechanical Shop

- Production of the mechanical elements used across all stages of the probe card manufacturing process
- The unit is also engaged in the production of highly innovative and customized machines, not available on the market, used in the production process

A wide range of highly innovative technologies

Advanced micromachining

Advanced laser cutting:
high accuracy and fast lead time

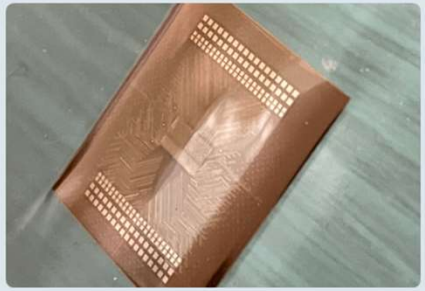


Thin film

Strong investment in advanced thin film technology to reduce lead time and improve quality and complexity

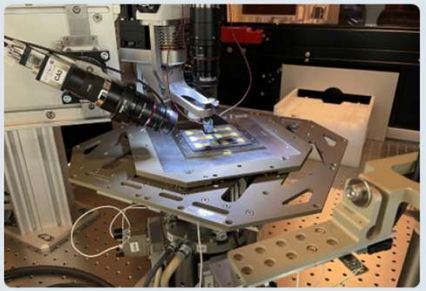
3D MEMS

Acquisition of MICROFABRICA in 2019; the sole company in the world specialized in 3D metallic MEMS manufacturing



Advanced manufacturing

Advanced manufacturing for high volume and best quality assembly of micro components



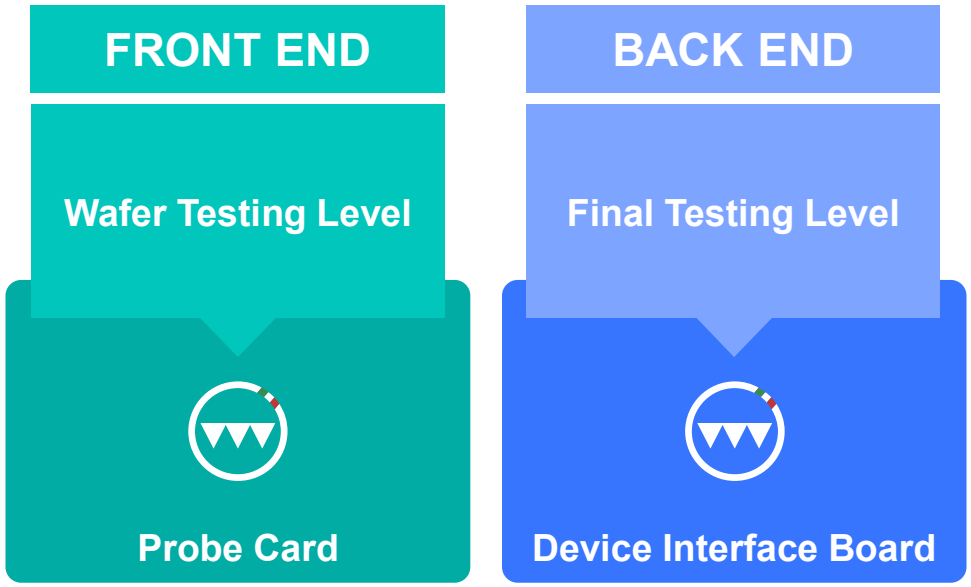
Vision & Strategy

INNOVATION BEGINS WITH US

Challenges & strategic setting

1	**Evolution of chip technology** **(more than Moore)** Scaling slow down as enabler for **chiplets**, **3D architectures** and **new materials**	→ **Continuous investments in R&D** → **M&A as accelerator of technological development**
2	**Increase in complexity** **Design and manufacturing** are becoming essential capabilities to reliably deliver **complex solutions**	→ **Strategic partnerships** → **Vertical integration of the most value-added components of the probe card**
3	**Client satisfaction** **Reliability** of the product & **on-time delivery**	→ **Support on site** → **Commercial agreements**

What’s next?


FRONT END
Wafer Testing Level
Probe Card
BACK END
Final Testing Level
Device Interface Board

What's next?

Consolidate the leading positioning in all test segments

FRONT END

Drive advancements in Logic Semiconductor Testing

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

Enter the High Bandwidth Memory (HBM) segment

BACK END

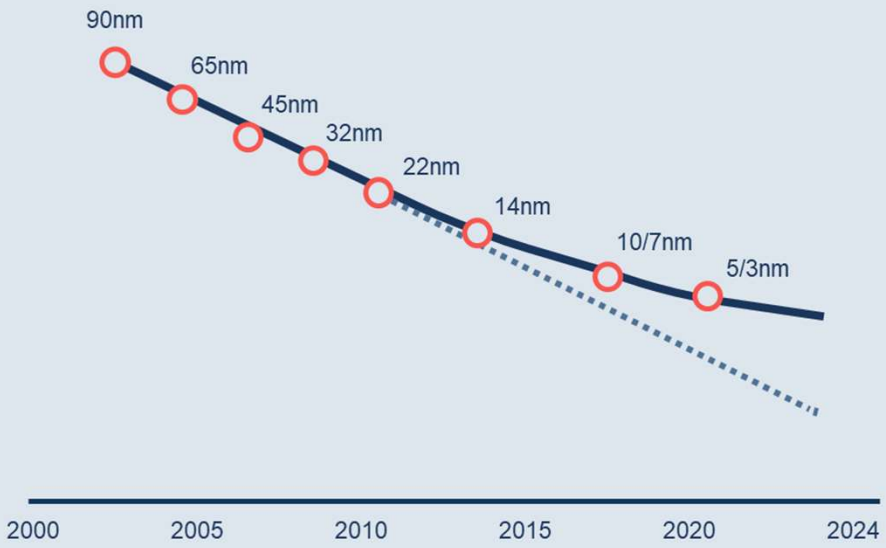
Strengthen positioning in Final Testing

Semiconductor technology trends

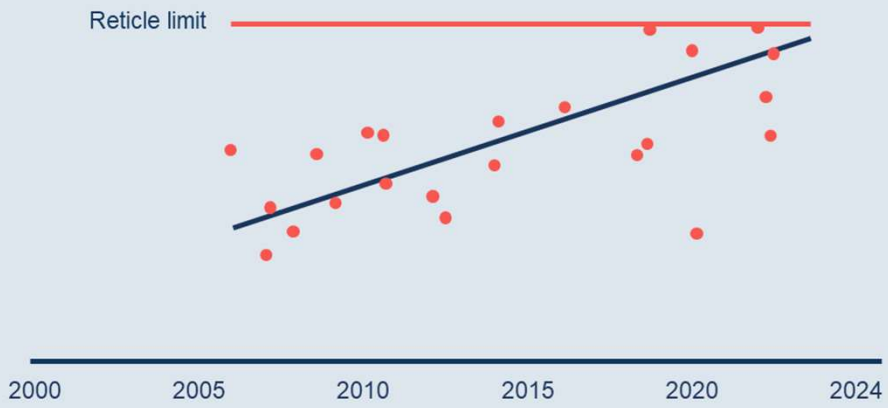
Industry motivation behind advanced packaging

How to continue drive for increase compute power in light of transistor density rate lower and die size growth limitations?

Transistor scaling rate is decreasing



Die size scaling limited by reticle size and yield optimization

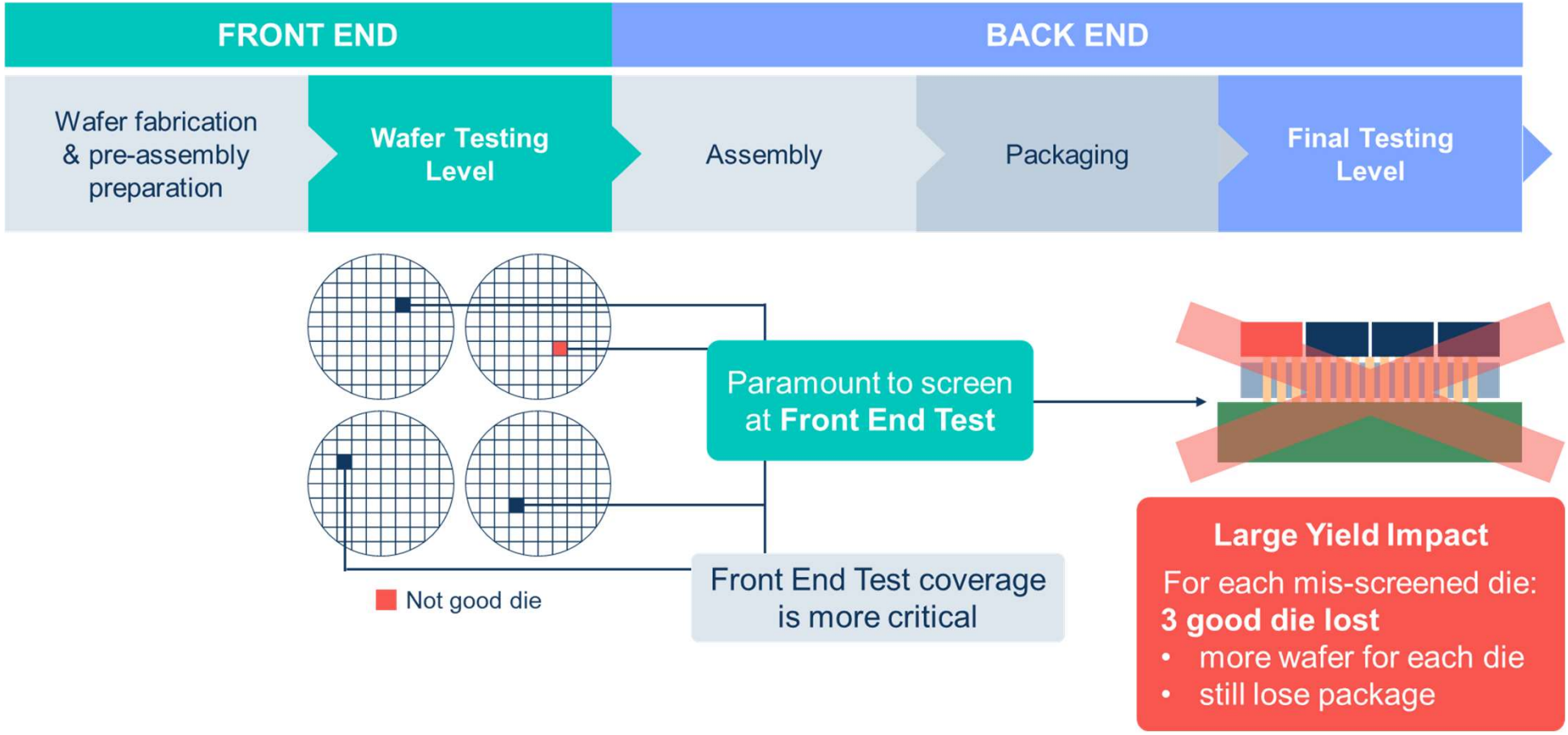


Semiconductor technology trends

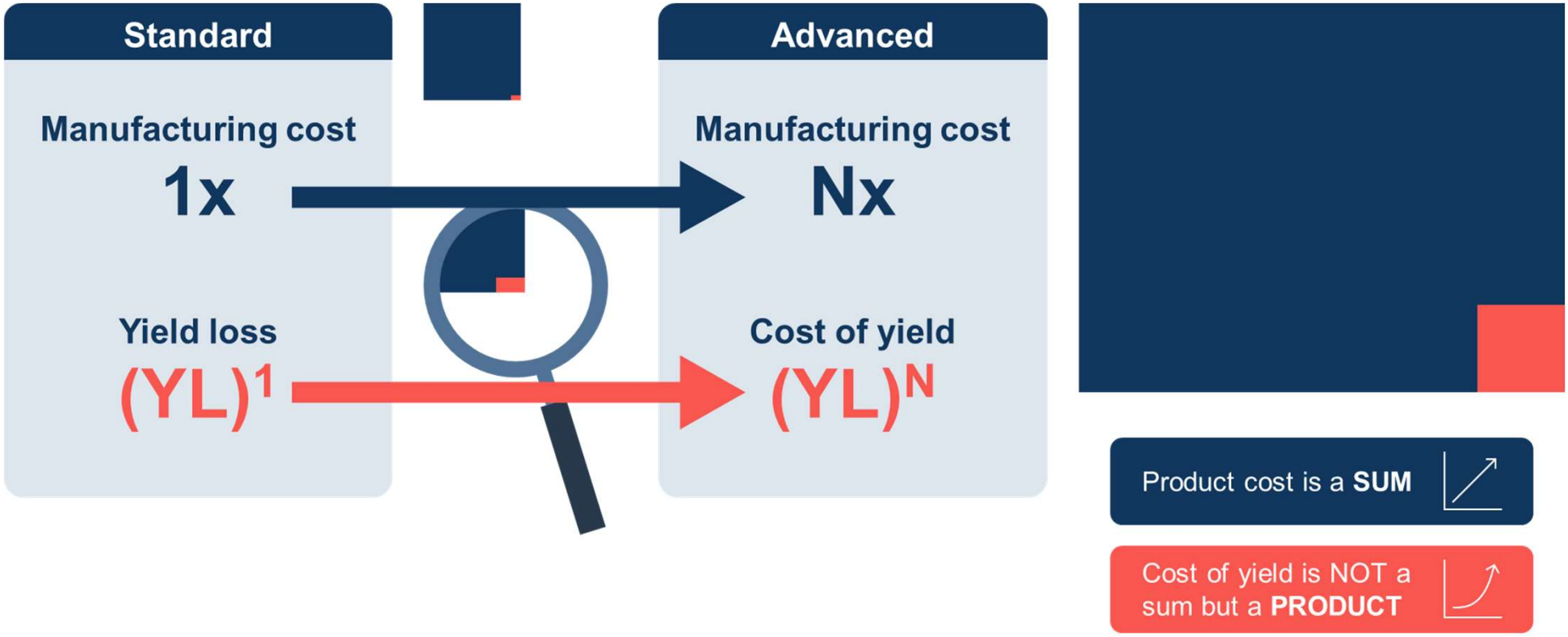
Solution: die disaggregation and advanced packaging

- Improved wafer-level yield with smaller chiplet
- Optimizing performance with mixed functionality capabilities
  - Memory
  - Co-packaged optics
- Allows for mixed technology node application and IP reuse

Semiconductor technology trends



Advanced packaging versus standard



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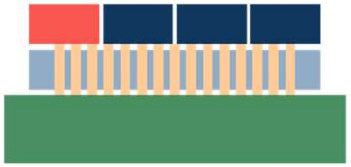


Front End Test coverage
is more critical

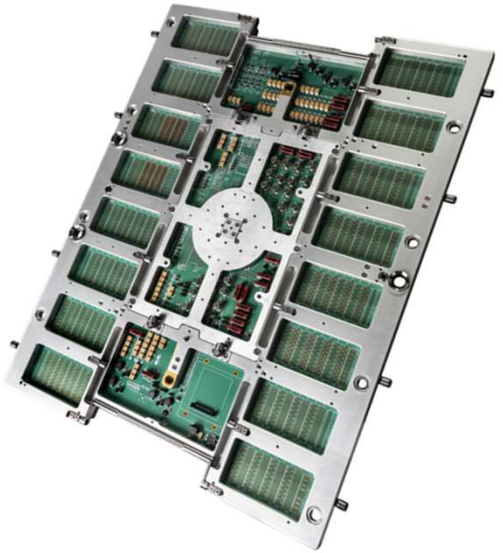
True **Known Good Die** required!

SOLUTION

more test at probe

=

more Probe Cards



Technoprobe as advanced packaging enabler

Fine pitch and ultra-large pin count

Necessary to effectively probe HPC and HBM's and all leading-edge product

High-speed

Short, ultra short and RF-specific needles technology to manage high speed interconnect IO, including SiPh

High power and thermal

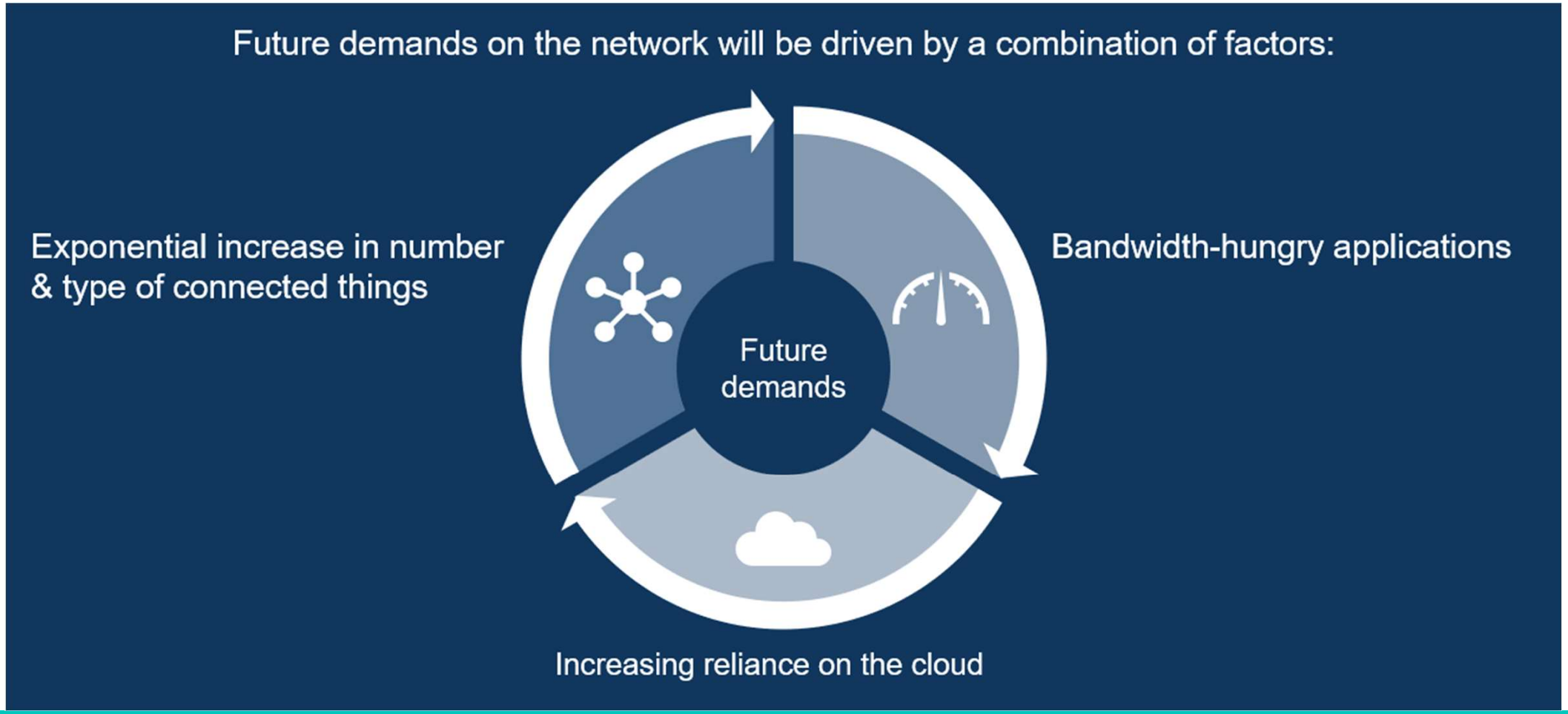
Delivering high power to DUT in effective and reliable way

Ability to remove heat dissipated by the probe card (directly or because of power transferred from DUT to PC)

High-density interconnect

Ultra-high complexity PCB and MLO/MLC for resource fan-out on ATE/SLT

A hungry world of wideband applications



FRONT END Proliferate high-speed, high-voltage, radio frequency and silicon photonics

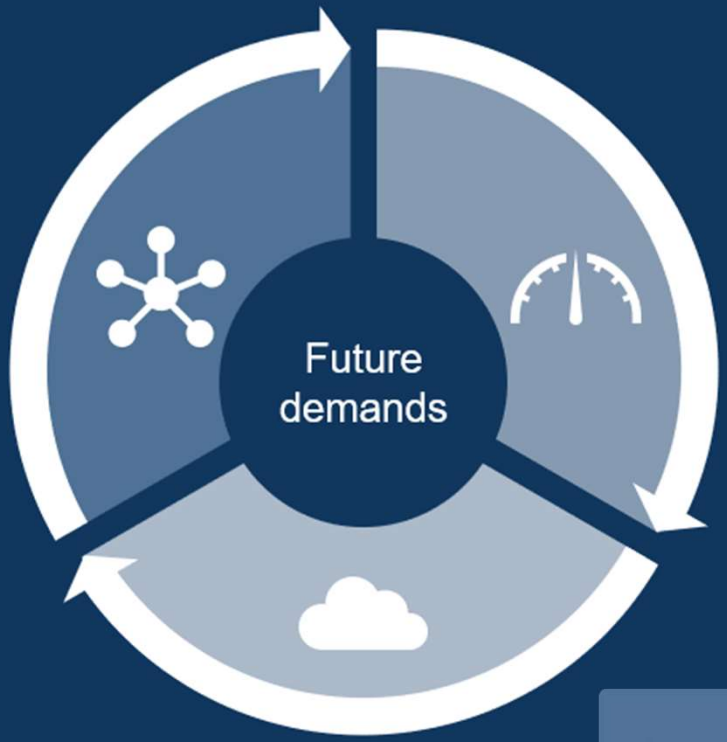
A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Proliferation of connections

Analog radio frequency

Satellite communications and sensing, automotive radar, mobile communication,…

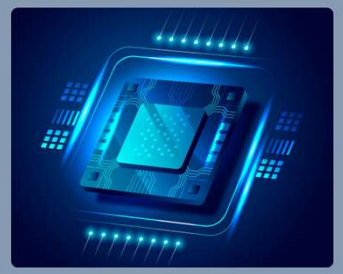


Increasing reliance on the cloud

Bandwidth - hungry applications

Silicon photonics

Chiplet to chiplet interconnect / photonics-driven computing



Chiplet probing

High density and high-speed IO inside chiplet demand for high-performance probe needles

FRONT END Proliferate high-speed, high-voltage, radio frequency and silicon photonics

A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

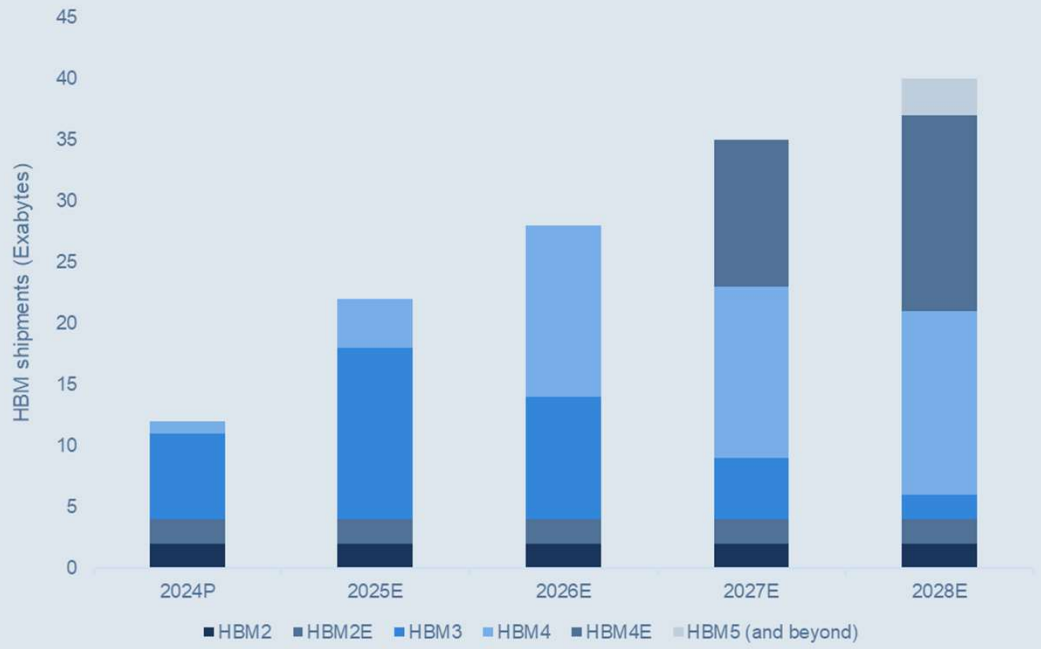
Silicon photonics

Technoprobe technologies integrated in the same product enable…

Fine pitch probing	→	alignment with advanced packaging roadmap
Radio frequency probes	→	high-speed performances in same probe card solutions
Technoprobe IP	→	usage of standard wafer prober
Integration of other IP from specific segment suppliers	→	flexibility and compliancy with customer preferred test method

FRONT END Proliferate high-speed, high-voltage, radio frequency and silicon photonics

DRAM & HBM: complexity as driver to new products



- **HBM demand continues to grow**
- **HBM bandwidth requirements almost double gen-gen**

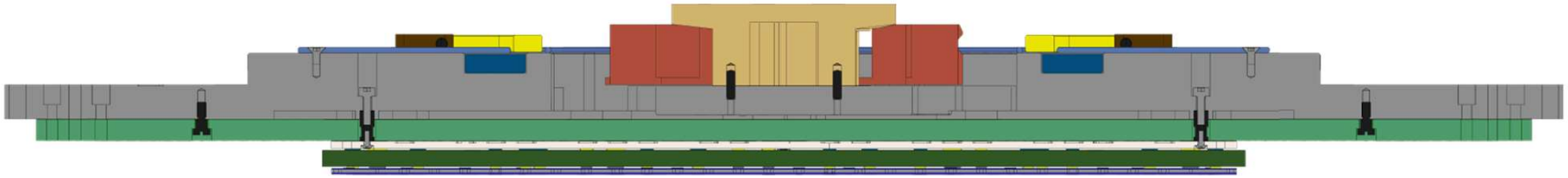
Source: Yole DRAM market monitor Q1 2025.

DRAM & HBM: complexity as driver to new products

DRAM and HBM are typically tested with **microcantilever** probing technologies.

Most **advanced HBM** and Next Generation products are becoming more challenging in terms of pad pitch, signal integrity, and power.

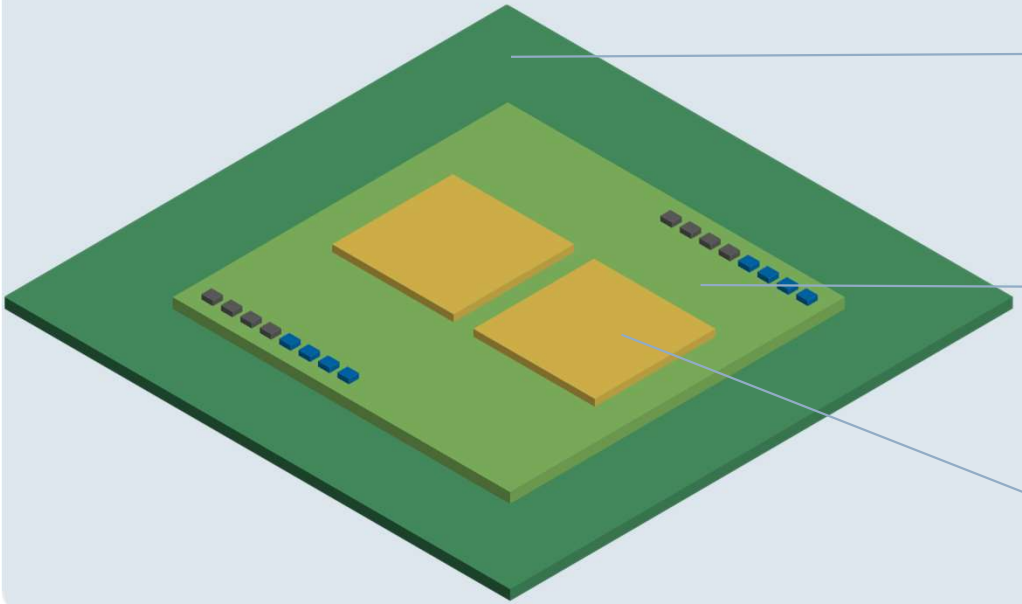
For both applications Technoprobe is leveraging on **Vertical MEMS** solution and on a unique PC architecture.



FusionLink

FUSIONLINK

We have applied the disaggregation to test interface hardware

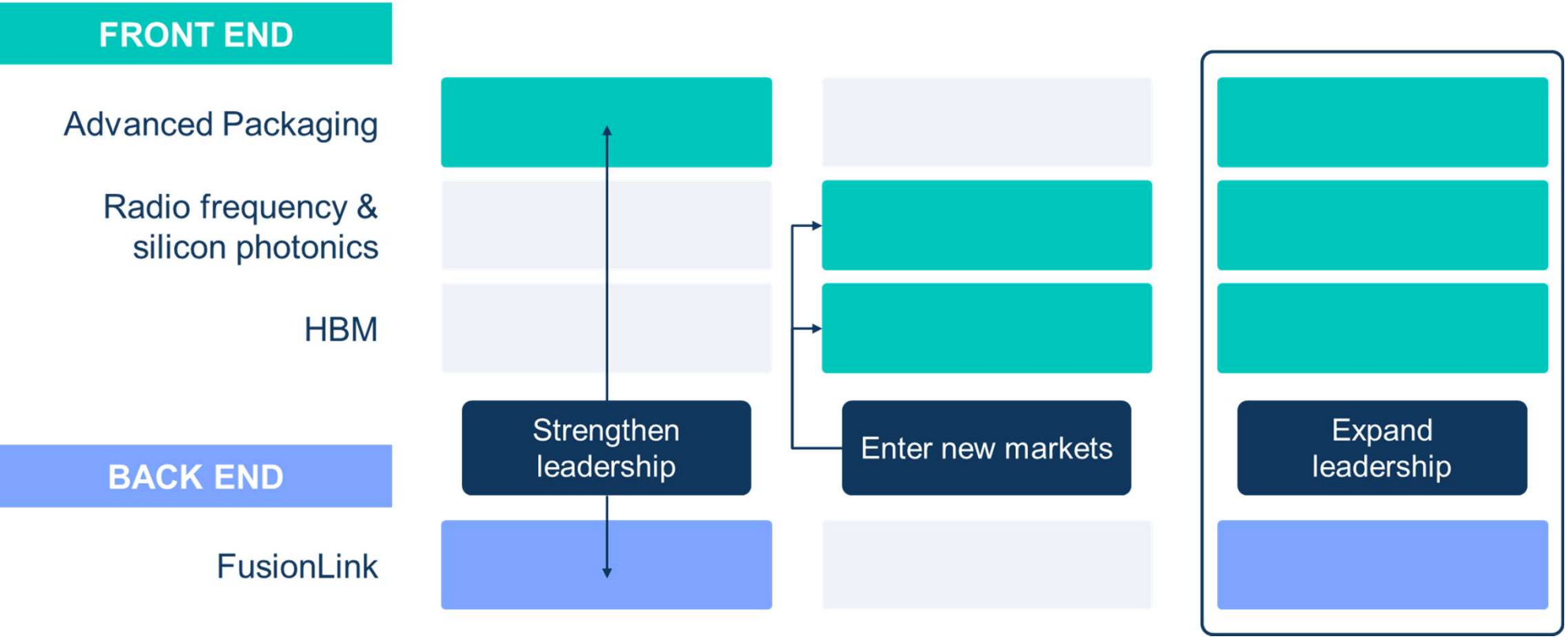


Main motherboard
Best technology: printed circuit board (PCB)

Device substrate
Best technology: high density interconnect (HDI)

Probe substrate
Best technology: multi-layer organic (MLO)

Growth drivers & trajectories

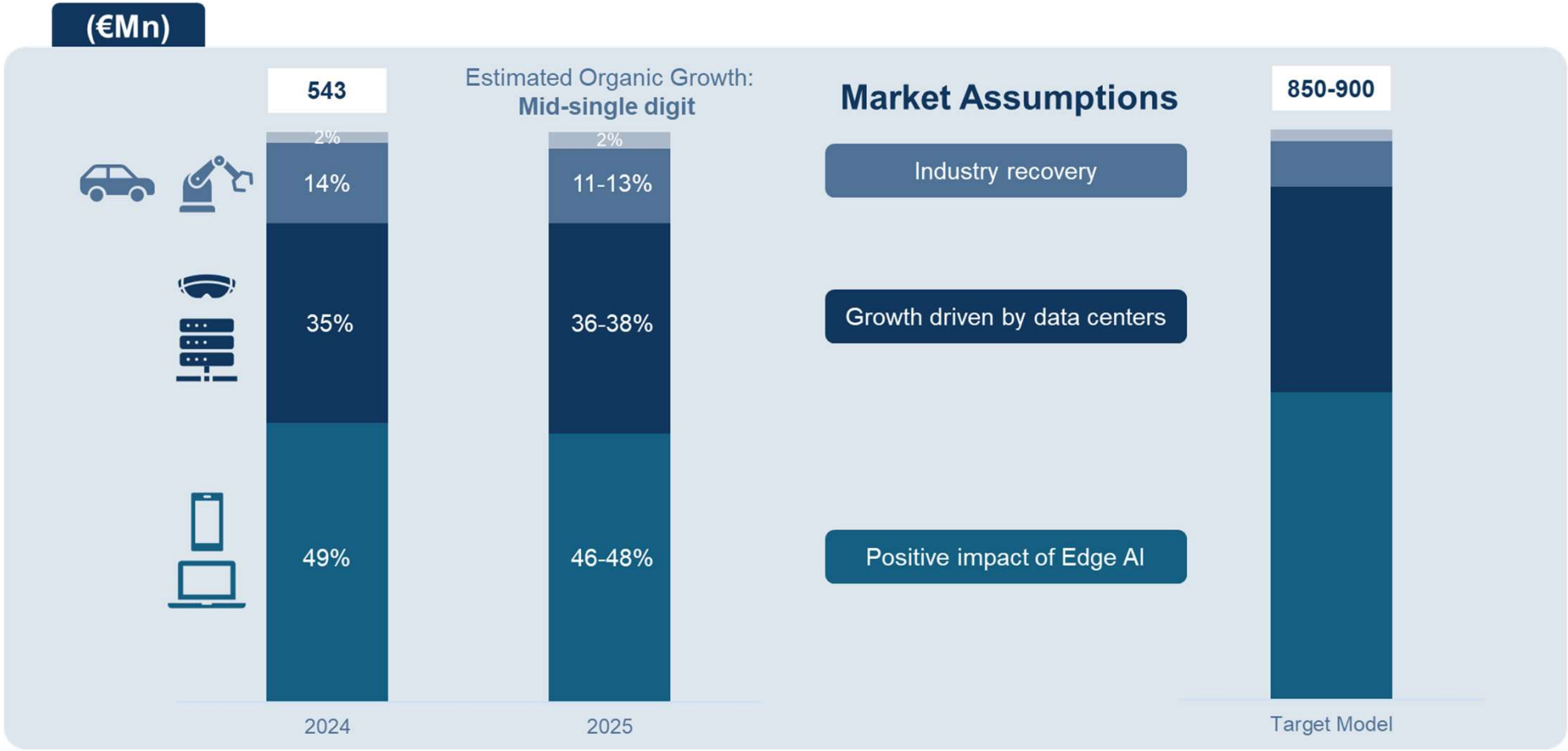


Financial Outlook

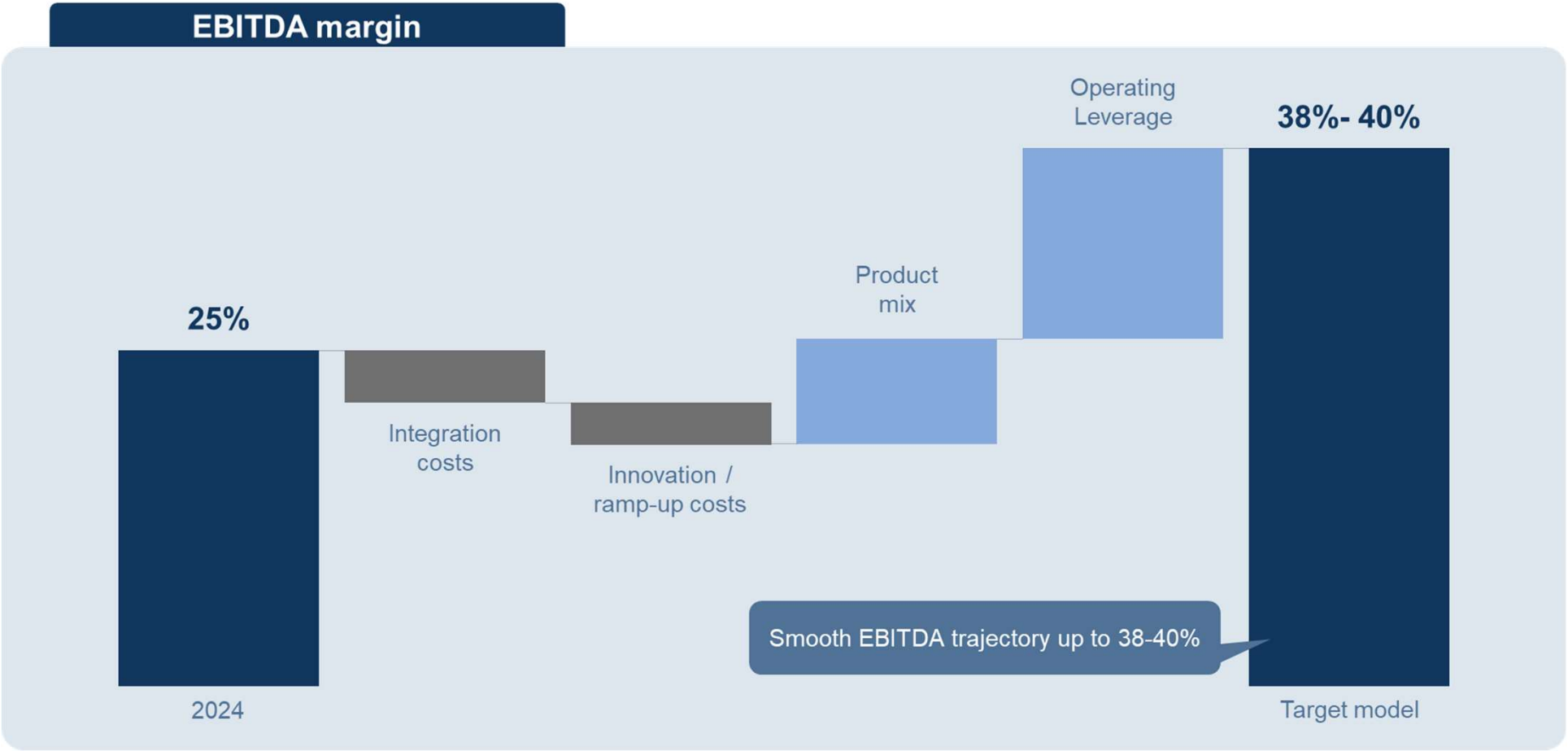
Mid-terms scenario

1	**Technological complexity evolution**	→ Testing solution for Advanced Packaging → Increase in demand for high-precision tests
2	**Market trends**	→ AI will lead the growth for many market segments → Expansion of memory semiconductor segments
3	**Geo-political instability**	→ Technological sovereignty → Commercial policies

Market trends & revenues path



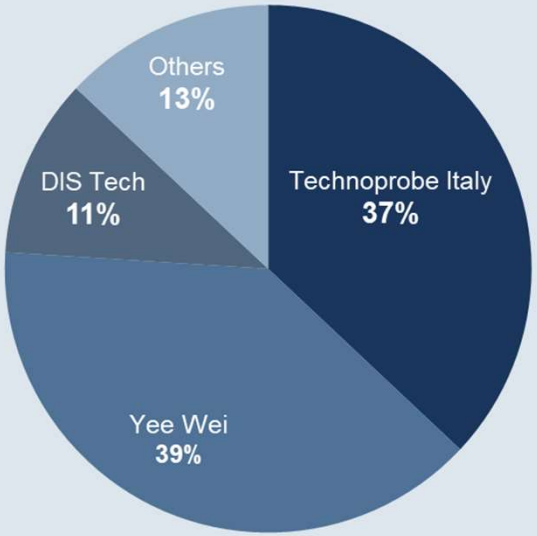
Profitability profile



Capex

(€Mn)

FY 2024



	FY 2022	FY 2023	FY 2024	Target Model
Revenues	549	409	543	
Capex	84	73	100	
Capex as % of Revenues	*15%*	*18%*	*18%*	*8% - 10%*

H1 2025 Results

INNOVATION BEGINS WITH US

H1 2025 Market Drivers

Revenues at **325.9€m**

up 7.3% QoQ
up 35.2% YoY


Consistent growth in AI


Slight increase in Consumer market


Weakness in Automotive only partially offset by upward trend in Industrial

Financial Highlights

Q2 2025

Revenues were **168.7€m**
up 21.1% YoY, up 7.3% QoQ

Gross Profit was **79.9€m**
up 38.4% YoY, with a margin of 47.3%

Ebitda was **58.3€m**
up 61.8% YoY, with a margin of 34.6%

H1 2025

Revenues were **325.9€m**
up 35.2% YoY

Gross Profit was **150.6€m**
up 49.5% YoY, with a margin of 46.2%

Ebitda was **106.4€m**
up 75.2% YoY, with a margin of 32.6%

Financial Highlights

€m	H1 2025	H1 2024	YoY Variance
Revenues	325.9	241.1	+35.2%
Gross profit	150.6	100.8	+49.5%
% margin	*46.2%*	*41.8%*	
EBITDA	106.4	60.7	+75.2%
% margin	*32.6%*	*25.2%*	

	30.06.2025	31.12.2024
Net Financial Position	641.9	656.3

Comments

- **Benefit** from:
  - Organic growth: rising trend in AI and slight increase in consumer, partially offset by shrinkage in auto and industrial
  - Change of perimeter (6 months of DIS revenue in H1'25 vs 1 month in H1'24)
- **Gross profit margin** benefitted from:
  - Recovered production efficiency
  - Operating leverage effect
- **Ebitda margin,** in addition to the above, benefitted also from US reorganization positive impact
- **Net financial position:** variance mainly attributable to solid cash flow from operating activities (+69€m), offset by capex (-28€m), the acquisition of a minority stake in Yee Wei Inc. (-20€m) and Innostar Service Inc. (-7€m), together with the unrealized fx impact on foreign currency bank accounts (-29€m).

Q3 2025 Guidance

Revenues: 137€m

(+/-3%)

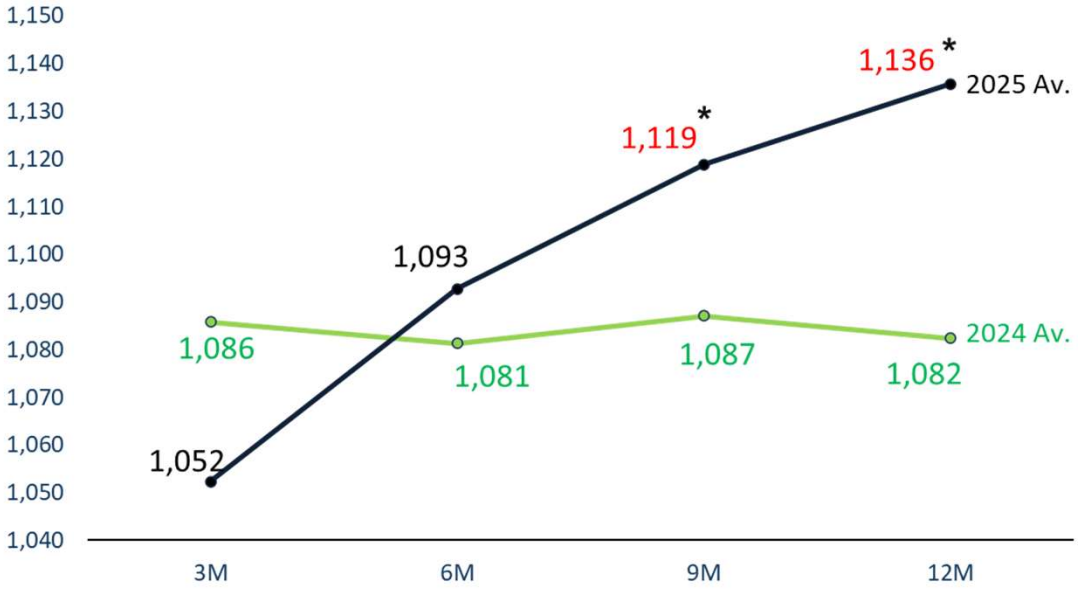
Gross Margin: 41.2%

(+/-2%)

Ebitda Margin: 28.2%

(+/-2%)

EUR/USD - Accumulated Average by Quarter



Average	Q1 '25	Q2 '25	Q3 '25*	Q4 '25*
	1,052	1,134	1,168	1,186
3M	**1,052**			
6M	**1,093**			
*9M**	**1,119**			
*12M**	**1,136**			

** Estimate*

Average	Q1 '24	Q2 '24	Q3 '24	Q4 '24
	1,086	1,077	1,098	1,068
3M	**1,086**			
6M	**1,081**			
9M	**1,087**			
12M	**1,082**			