14th April 2025

Capital Market Day 2025

TECHNOPROBE

Disclaimer

This document has been prepared by Technoprobe S.p.A. (the "Company") solely for use in the presentation of the Technoprobe Group (the "Group") and its financial results.

This document does not constitute or form part of any offer or invitation to sell, or any solicitation to purchase any security issued by the Company. The information contained and the opinions expressed in this document have not been independently verified. In particular, this document may contain forward-looking statements that are based on current estimates and assumptions made by the management of the Company to the best of its knowledge. Such forward-looking statements are subject to risks and uncertainties, the non-occurrence or occurrence of which could cause the actual results–including the financial condition and profitability of the Group– to differ materially from or be more negative than those expressed or implied by such forward-looking statements.
This also applies to the forward-looking estimates and forecasts derived from third-party studies. Consequently, neither the Company nor its management can give any assurance regarding the future accuracy of the estimates of future performance set forth in this document or the actual occurrence of the predicted developments. Stefano Beretta, as the officer in charge of preparing the corporate accounting documents, declares in accordance with paragraph 2, Article 154-bis of Legislative Decree No. 58/1998 ("Consolidated Finance Act"), that the accounting information included in this presentation corresponds to the underlying accounting records, and ii) in accordance with paragraph 5-ter, Article 154-bis of the Consolidated Finance Act.

This document makes use of some alternative performance indicators. The management of the Company considers these indicators key parameters to monitor the Group's economic and financial performance. As the represented indicators are not identified as accounting measurements according to IFRS standards, the Group calculation criteria may not be uniform with those adopted by other groups and, therefore, may not be comparable.

The data and information contained in this document are subject to variations and integrations. Although the Company reserves the right to make such variations and integrations when it deems necessary or appropriate, the Company assumes no affirmative disclosure obligation to make such variations and integrations.

Agenda

Capital Market Day 2025

01 | **Our Vision & Strategy**
Stefano Felici - CEO

02 | **Market Perspective**
Marco Prea - CCO

03 | **Technology & Testing**
Joe Parks - CTO

04 | **Financial Outlook**
Stefano Beretta - CFO

Agenda

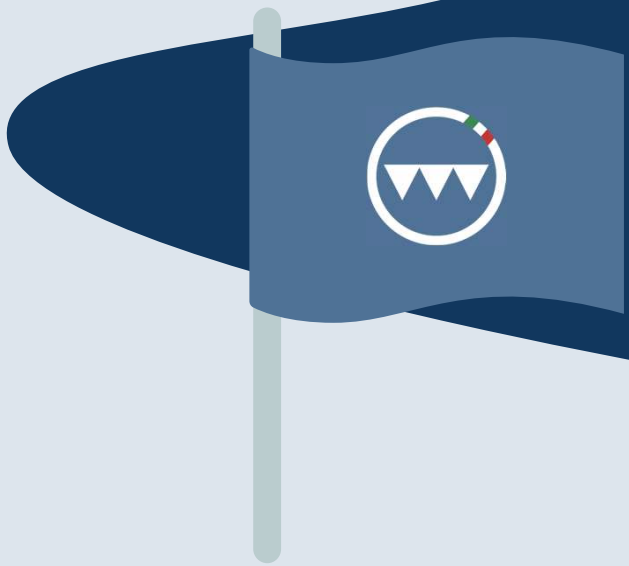
01 | **Our Vision & Strategy**

Stefano Felici - CEO

Capital Market Day 2025

So far so good

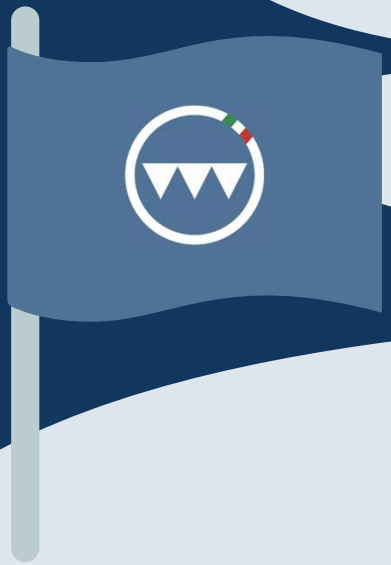
Leading player in designing & manufacturing of MEMS **Probe Cards** for logic chips



60%
2024 Market Share

So far so good

Customer satisfaction and **reputation** as cornerstone values



intel

Intel's 2025 EPIC Supplier Award

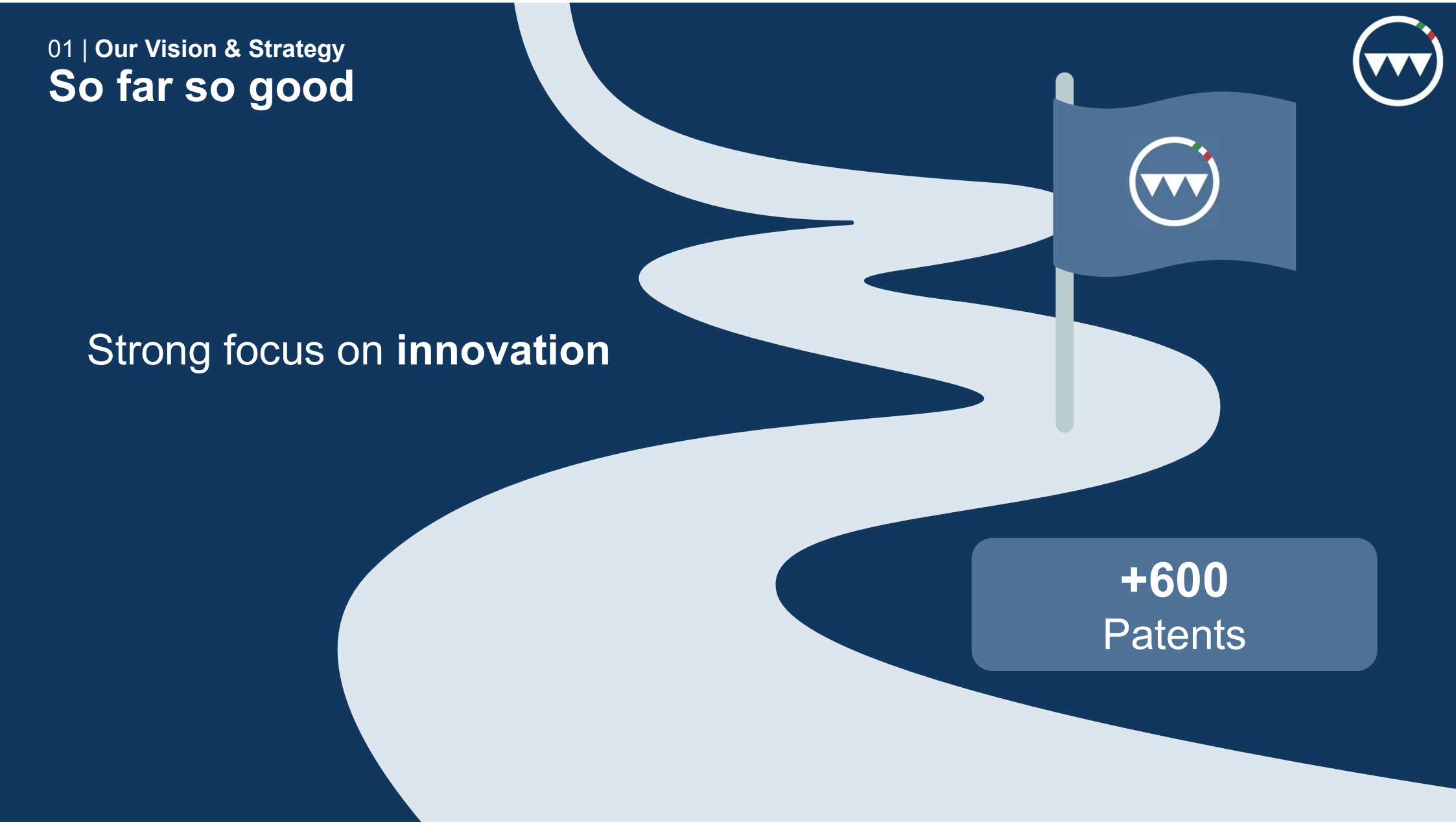
NEW

TSMC's Excellent Performance Award 2024

tsmc

So far so good

Strong focus on **innovation**

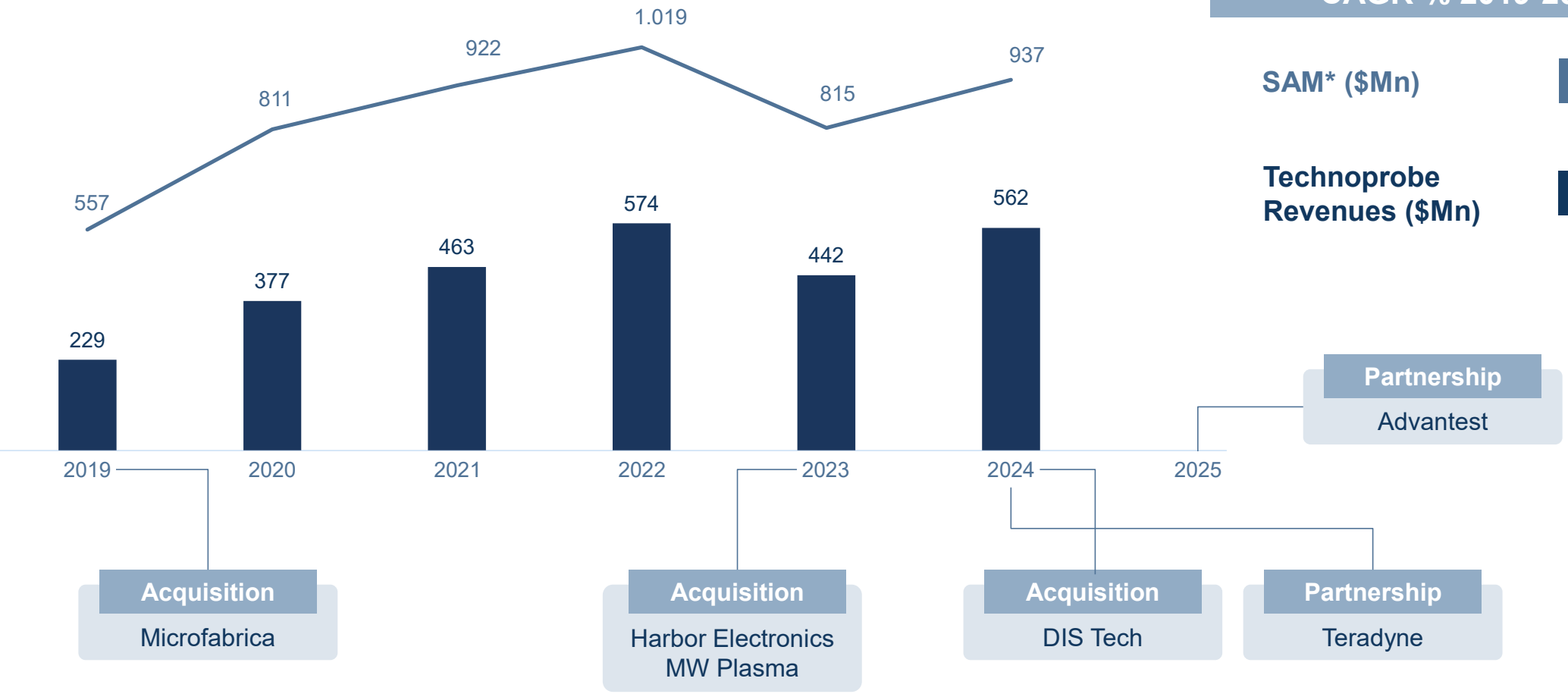


+600
Patents

So far so good

Extensive **global presence**
and widespread **local footprint**

Technoprobe evolution



CAGR % 2019-2024	
SAM* ($Mn)	+11%
Technoprobe Revenues ($Mn)	+20%

SAM*: MEMS Logic Probe Cards – Do not include Final Testing Market. Consistently, 2024 Revenues do not include Final Test for USD28m.
Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.
Revenues USD @ average annual exchange rate (CAGR €: +21.6%).

Our positioning in the testing space

FRONT END

Wafer fabrication & pre-assembly preparation

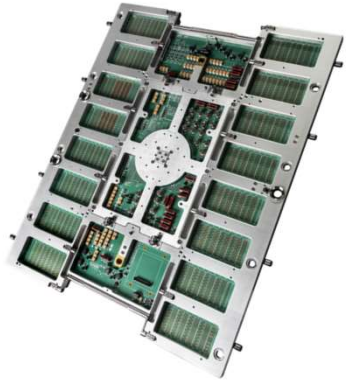
Wafer Testing Level

Wafer Level

Singulated Die

Advanced Packaging

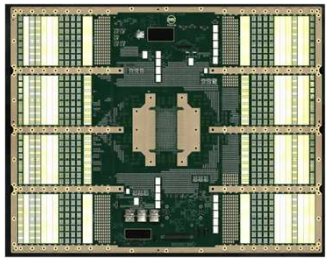
Probe Card



BACK END

Assembly

Packaging



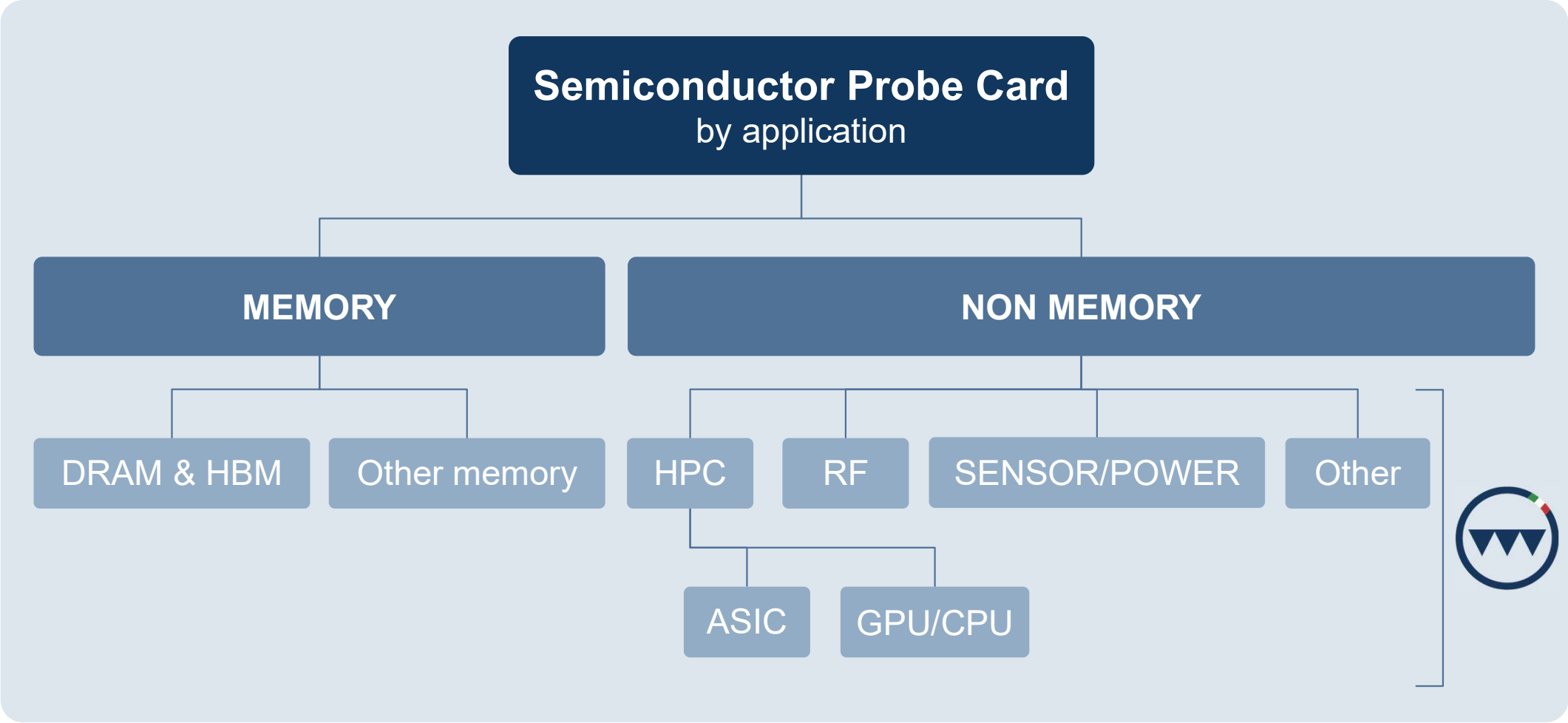
Final Testing Level

Socket

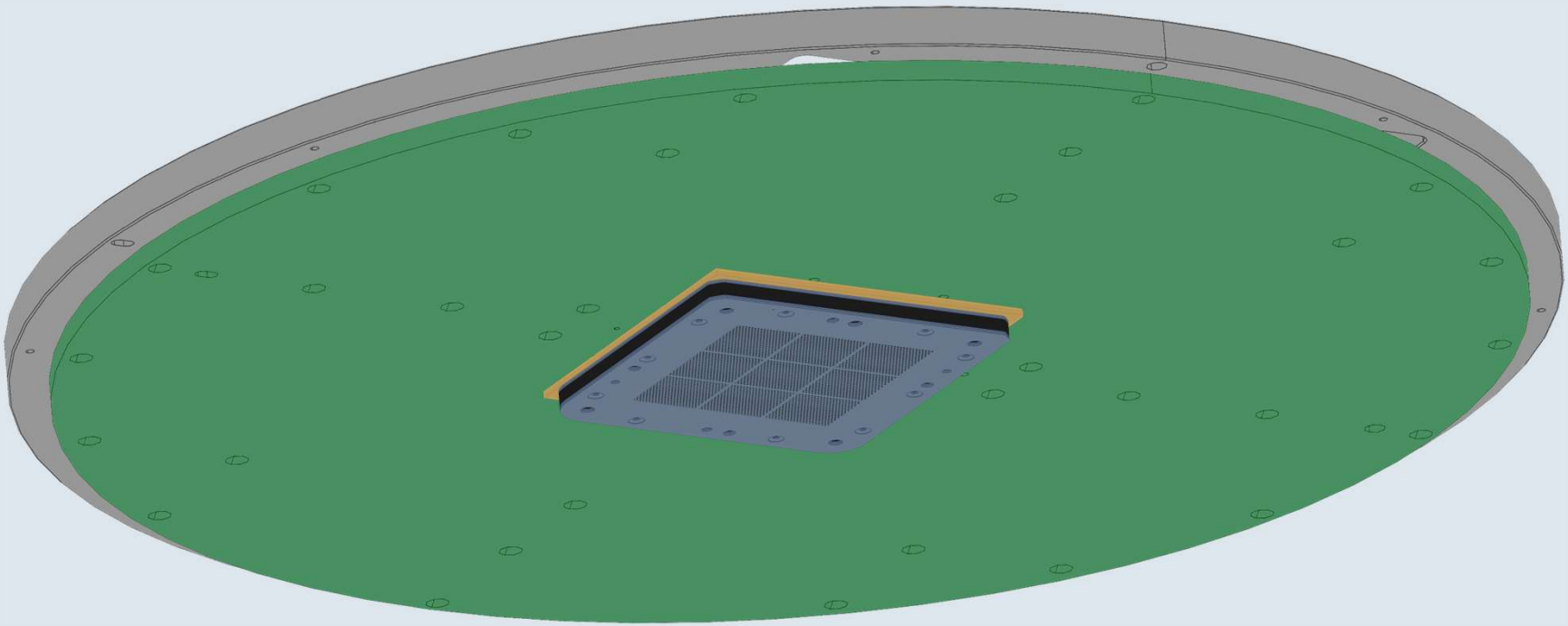
System Level Testing

Device Interface Board

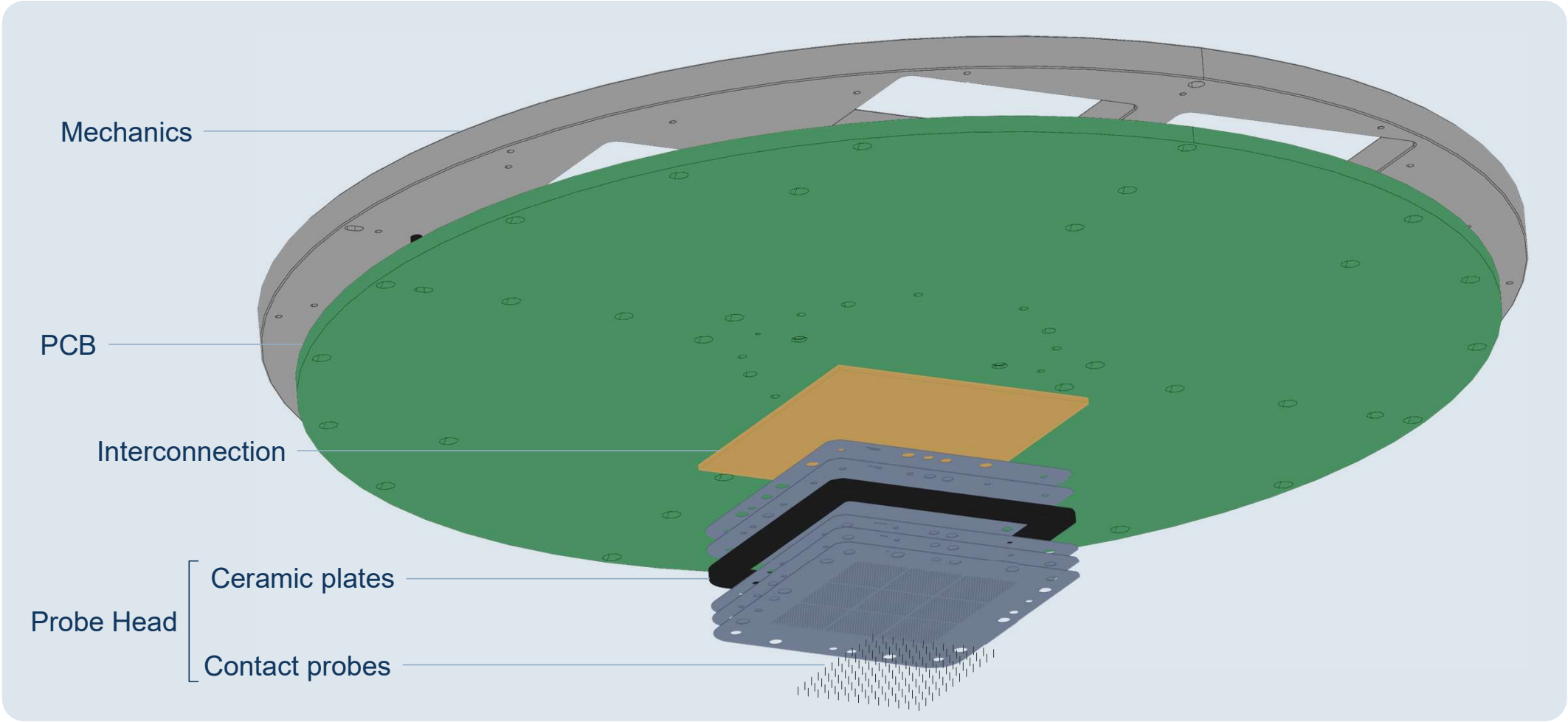
Our positioning in the semiconductor Probe Card market



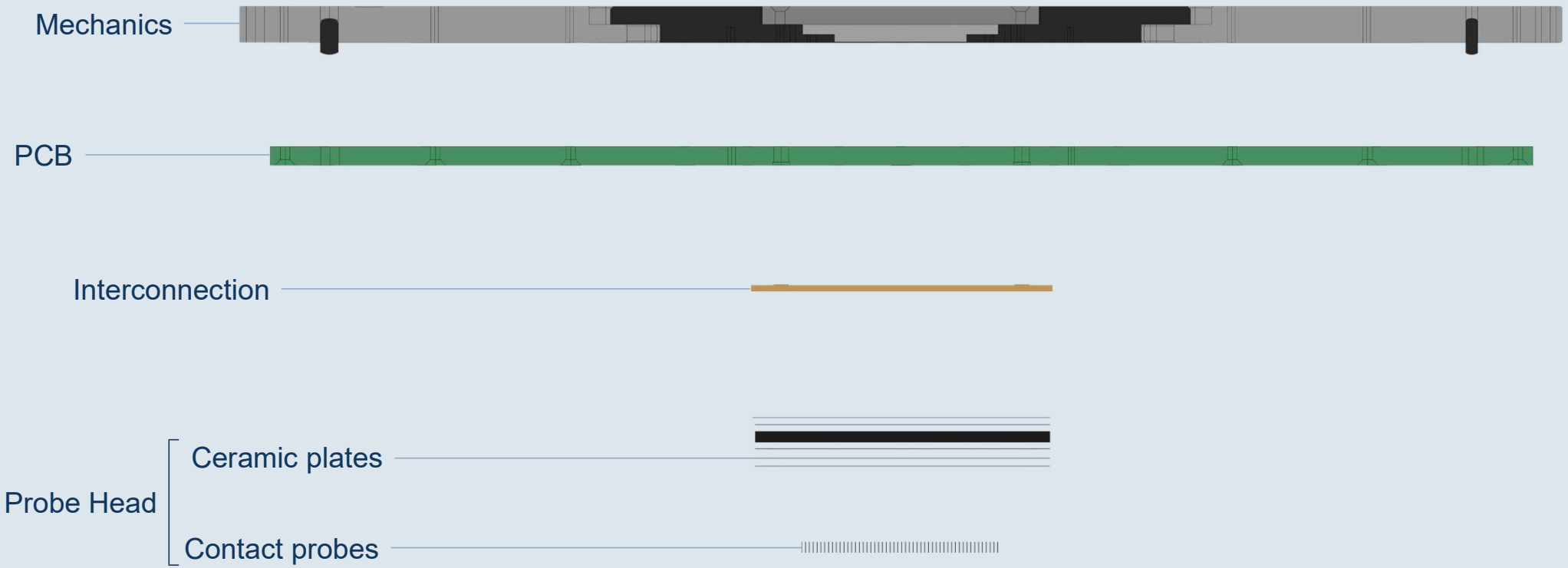
The Probe Card



The Probe Card



The Probe Card



Our business model

		Design	Manufacturing	Assembly
Wafer Testing Level				
Mechanics		✓	✓	✓
PCB		✓	Manufacturing partners & other suppliers	✓
Interconnection		✓	✓	✓
Probe head Ceramic plates Contact probes		✓	✓	✓
Final Testing Level				
Device Interface Boards		✓	Manufacturing partners & other suppliers	✓

Built an open eco-system partnerships

TERADYNE

Accelerate growth of complete Probe Card and Final Test Interfaces by acquisition of DIS

Joint Development Projects to deliver superior customer value in SOC and Memory

TECHNOPROBE

ADVANTEST

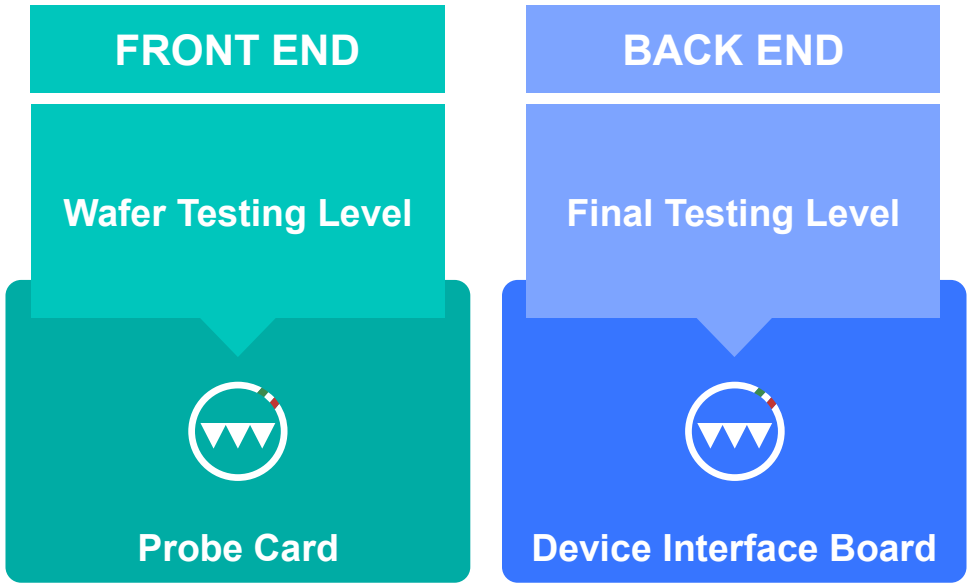
Priority suppliers of PCB

Joint Development Projects to share knowledge

Challenges & strategic setting

1	**Evolution of chip technology** **(more than Moore)** Scaling slow down as enabler for **chiplets**, **3D architectures** and **new materials**	→ **Continuous investments in R&D** → **M&A as accelerator of technological development**
2	**Increase in complexity** **Design and manufacturing** are becoming essential capabilities to reliably deliver **complex solutions**	→ **Strategic partnerships** → **Vertical integration of the most value-added components of the probe card**
3	**Client satisfaction** **Reliability** of the product & **on-time delivery**	→ **Support on site** → **Commercial agreements**

What’s next?


FRONT END
Wafer Testing Level
Probe Card
BACK END
Final Testing Level
Device Interface Board

What's next?

Consolidate the leading positioning in all test segments

FRONT END

Drive advancements in Logic Semiconductor Testing

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

Enter the High Bandwidth Memory (HBM) segment

BACK END

Strengthen positioning in Final Testing

Agenda

Capital Market Day 2025

01 | **Our Vision & Strategy**
Stefano Felici - CEO

02 | **Market perspective**
Marco Prea - CCO

03 | **Technology & Testing**
Joe Parks - CTO

04 | **Mid-term Plan**
Stefano Beretta - CFO

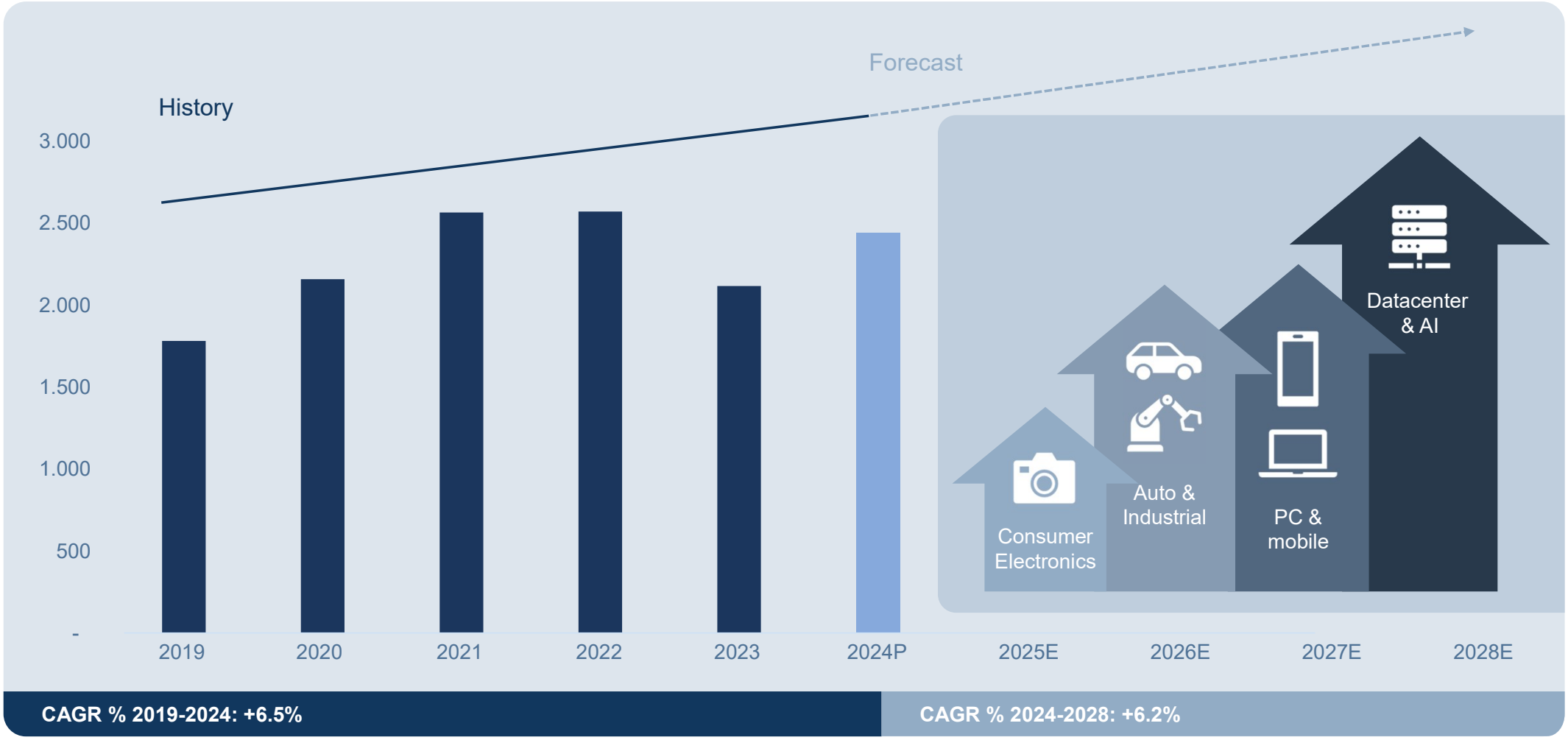
Agenda

02 | **Market Perspective**

Marco Prea - CCO

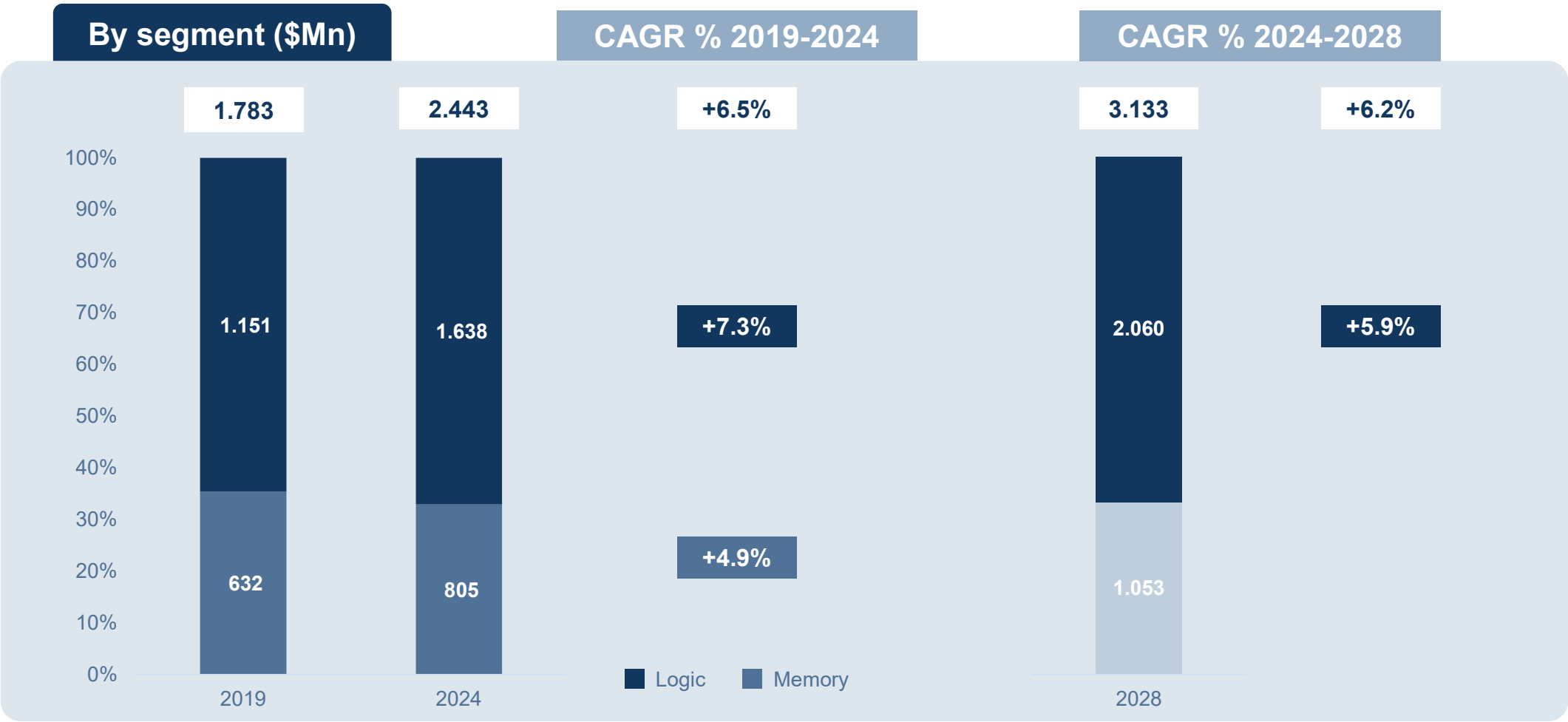
Capital Market Day 2025

The Probe Card market ($Mn)



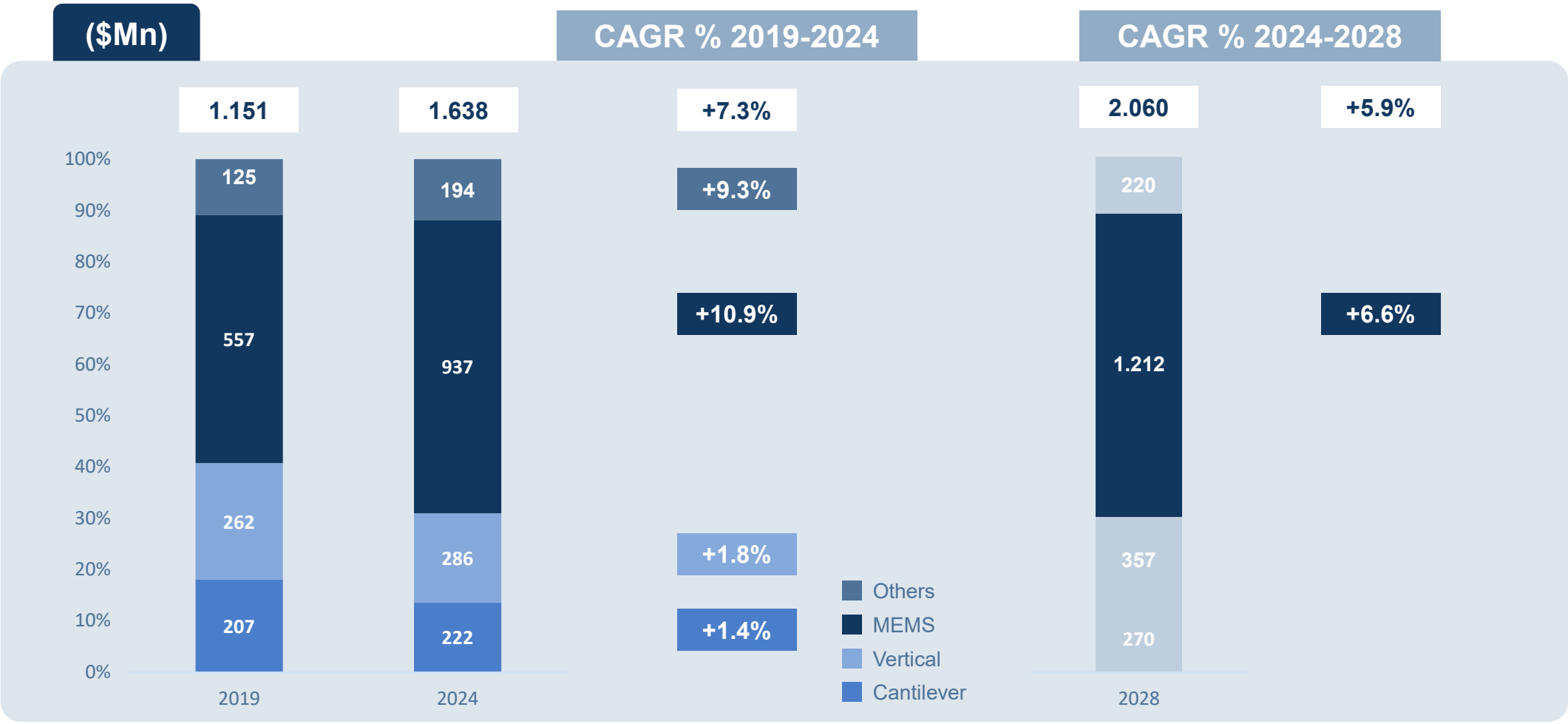
Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.

The Probe Card market



Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures. Memory: DRAM+NVM & Other memory. Logic: MEMS, Power, RF, CMOS Image Sensors, Photonics, Other non-memory, WAT.

Logic Probe Card by technology

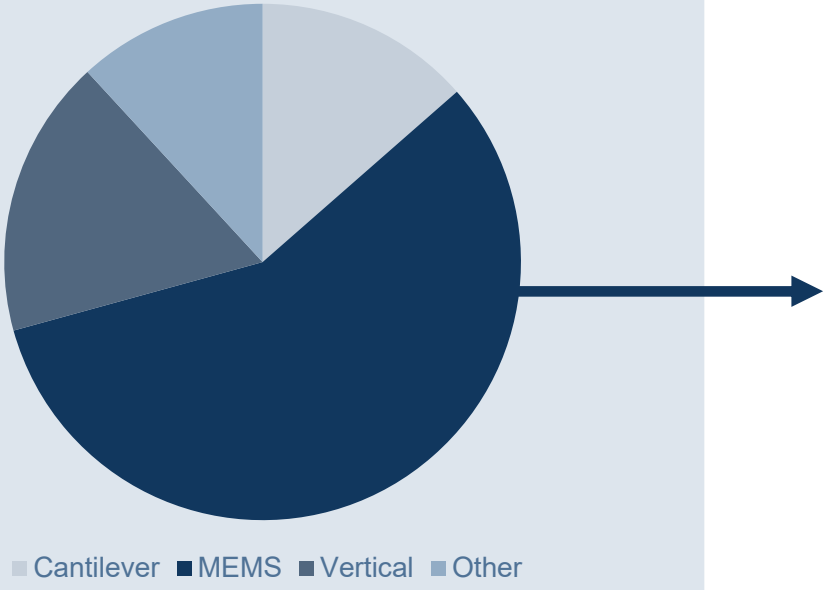


Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.

Our reference markets

2024 Logic Probe Card market

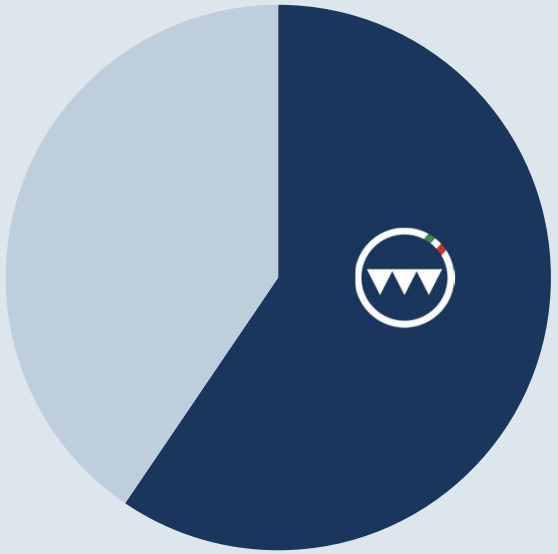
$1,6 Bn



Market Share: 34%

2024 MEMS Logic Probe Card

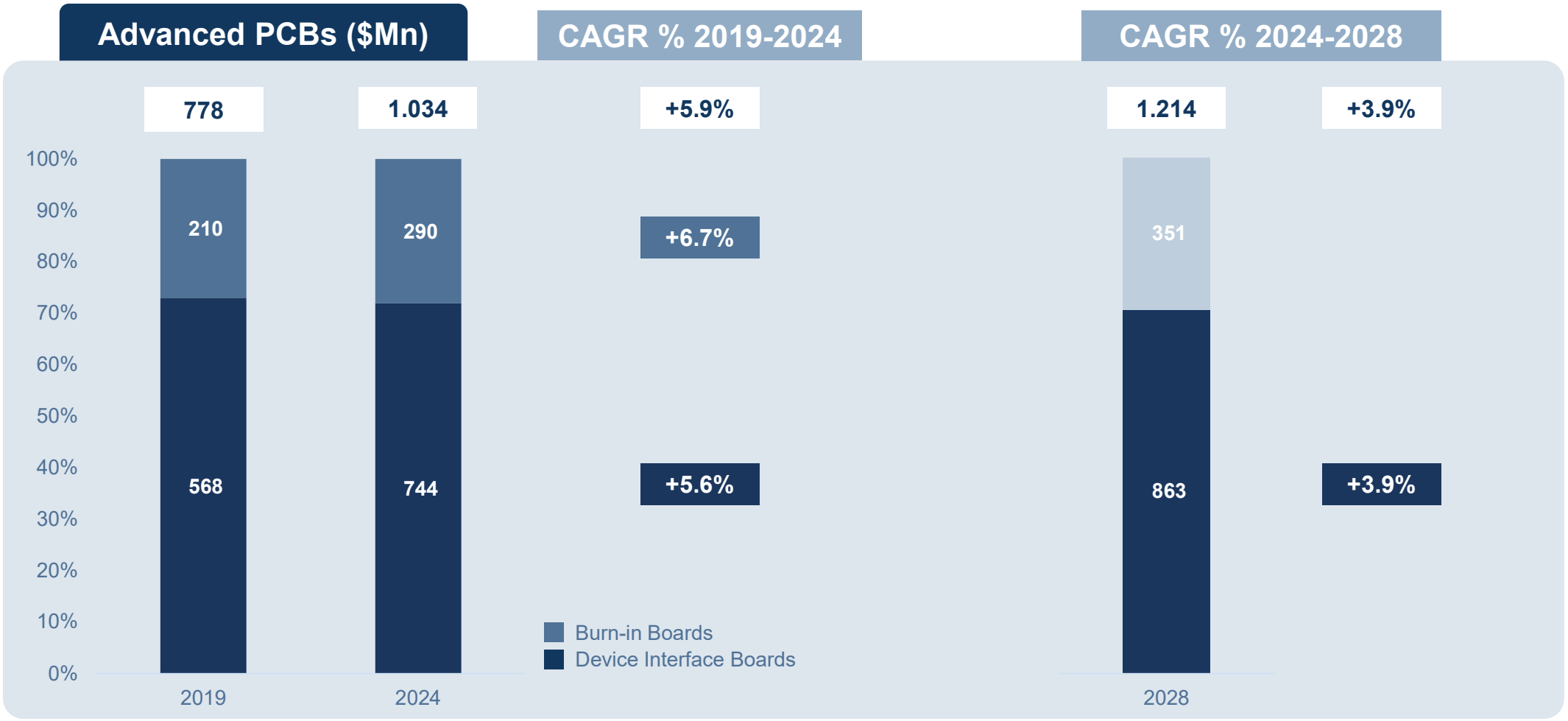
$937 Mn



Market Share: 60%

Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept.2024) – rounded figures.

Final Testing market – Advanced PCBs

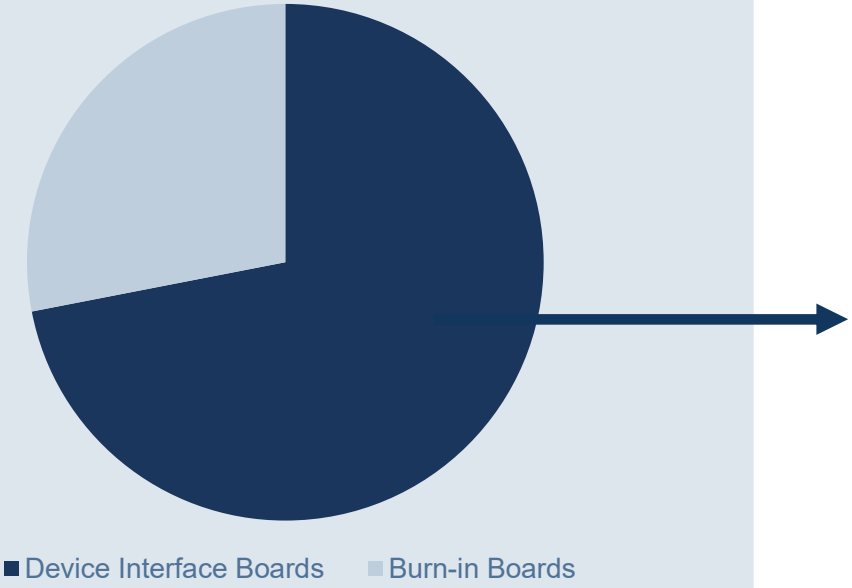


Source: Yole Test Interface Board market monitor Q3 2024 (Sept.2024) – rounded figures.

Our reference markets

2024 Advanced PCB for semiconductor

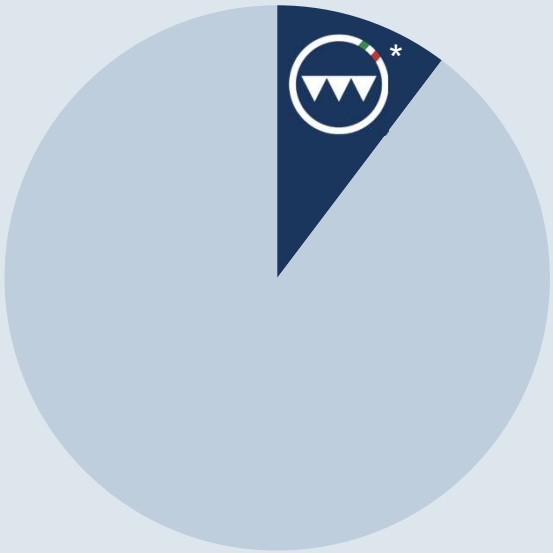
$1 Bn



Market Share: 6%

2024 Final Test DIB market

$744 Mn

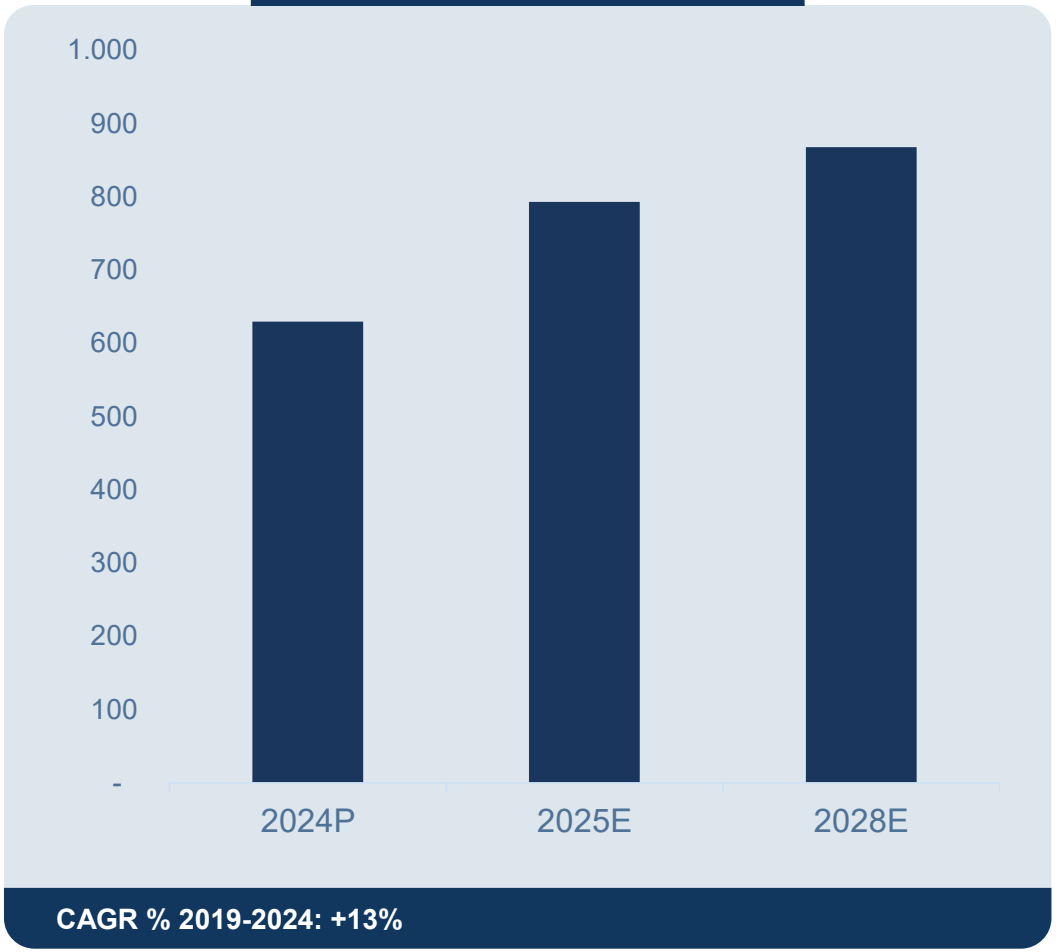


Market Share*: 8%

Source:Yole Test Interface Board market monitor Q3 2024 (Sept.2024) – rounded figures.
(*) Based on DIS Tech Final Test FY24 data. Company acquired by Technoprobe on May 27, 2024.

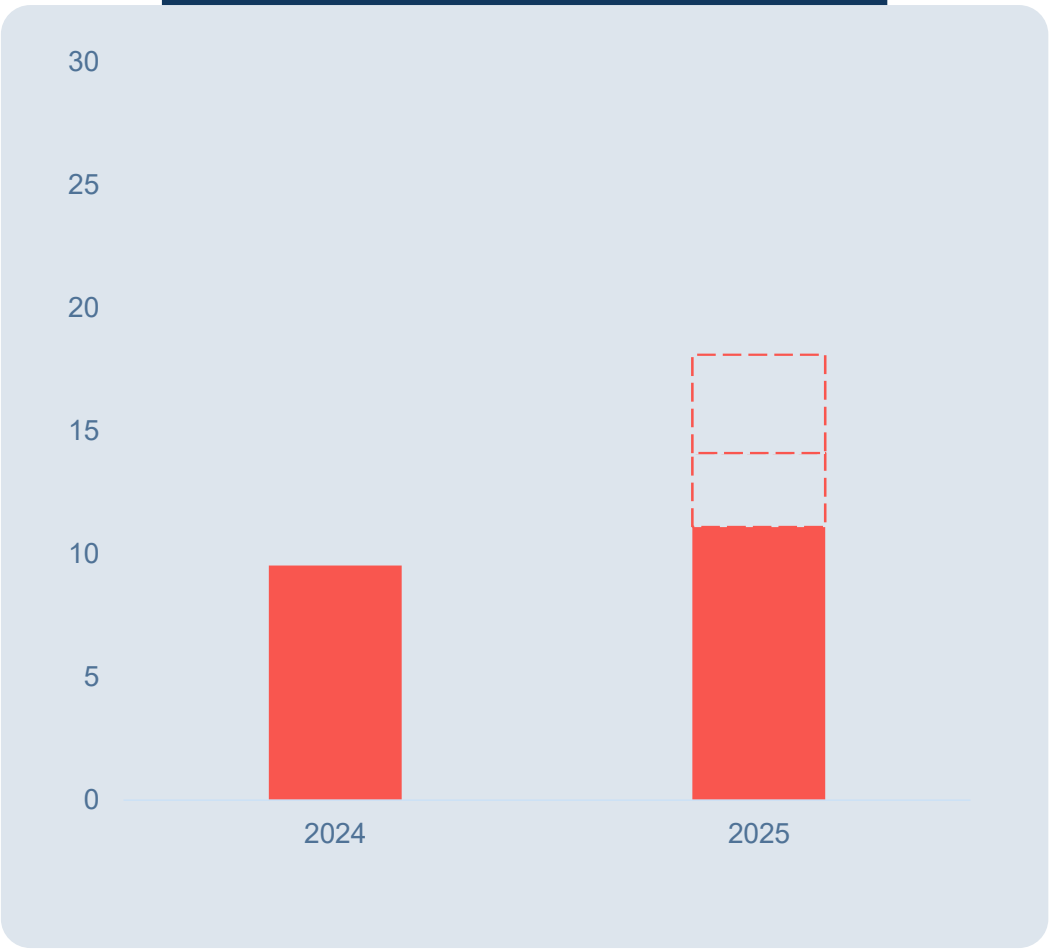
Focus on Memory market

Semiconductor market ($Bn)



CAGR % 2019-2024: +13%

Next Generation Memory market ($Bn)



Source: Yole and Precedence Research Estimates.

Key messages

MEMS Logic PC

Ever-growing market for leading edge technology

Key positioning on technological advances

Final Test

Immediate exposure to an expanded SAM

Technological breakthroughs from FusionLink

HBM

New challenge & opportunity

MEMS technology as a potential game changer

Agenda

Capital Market Day 2025

01 | **Our Vision & Strategy**
Stefano Felici - CEO

02 | **Market Perspective**
Marco Prea - CCO

03 | **Technology & Testing**
Joe Parks - CTO

04 | **Financial Outlook**
Stefano Beretta - CFO

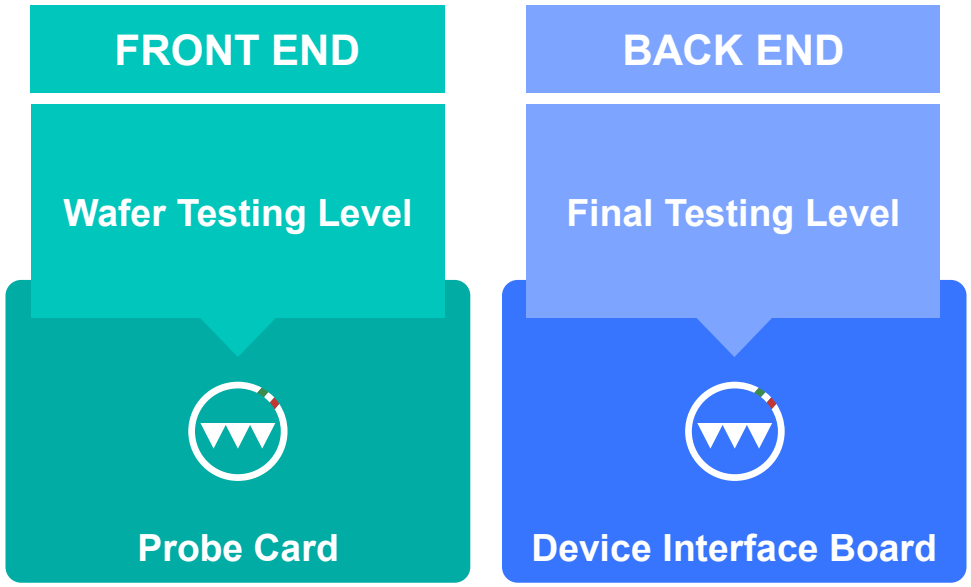
Agenda

03 | Technology & Testing

Joe Parks - CTO

Capital Market Day 2025

Growth drivers & trajectories



Growth drivers & trajectories

FRONT END

Drive advancements in Logic Semiconductor Testing

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

Enter the High Bandwidth Memory (HBM) segment

BACK END

Strengthen positioning in Final Testing

Growth drivers & trajectories

FRONT END

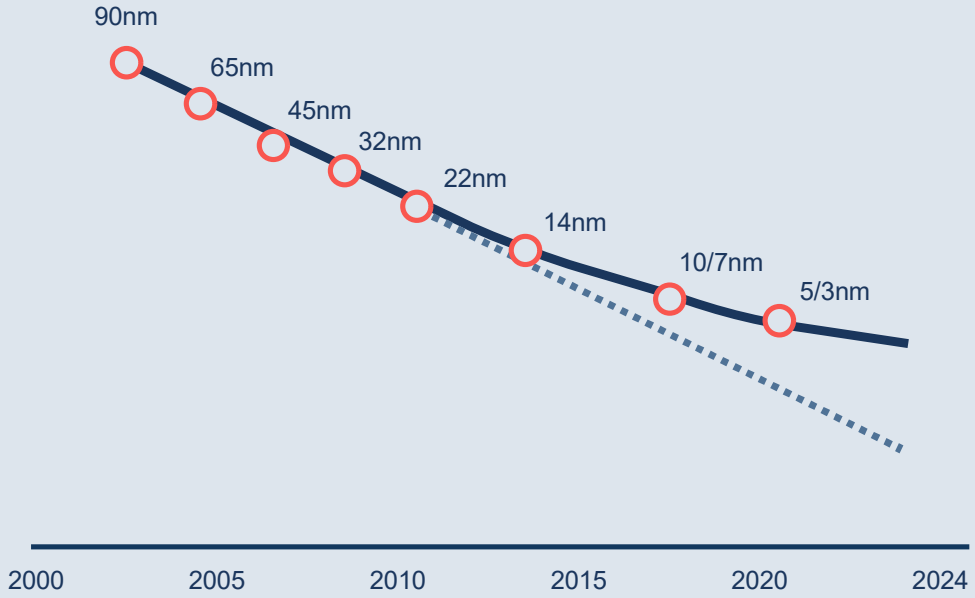
Drive advancements in Logic Semiconductor Testing

Semiconductor technology trend

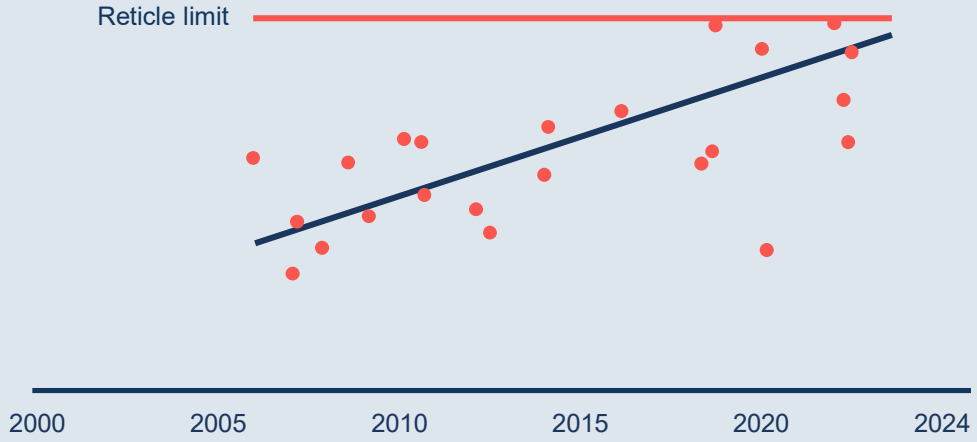
Industry motivation behind advanced packaging

How to continue drive for increase compute power in light of transistor density rate lower and die size growth limitations?

Transistor scaling rate is decreasing

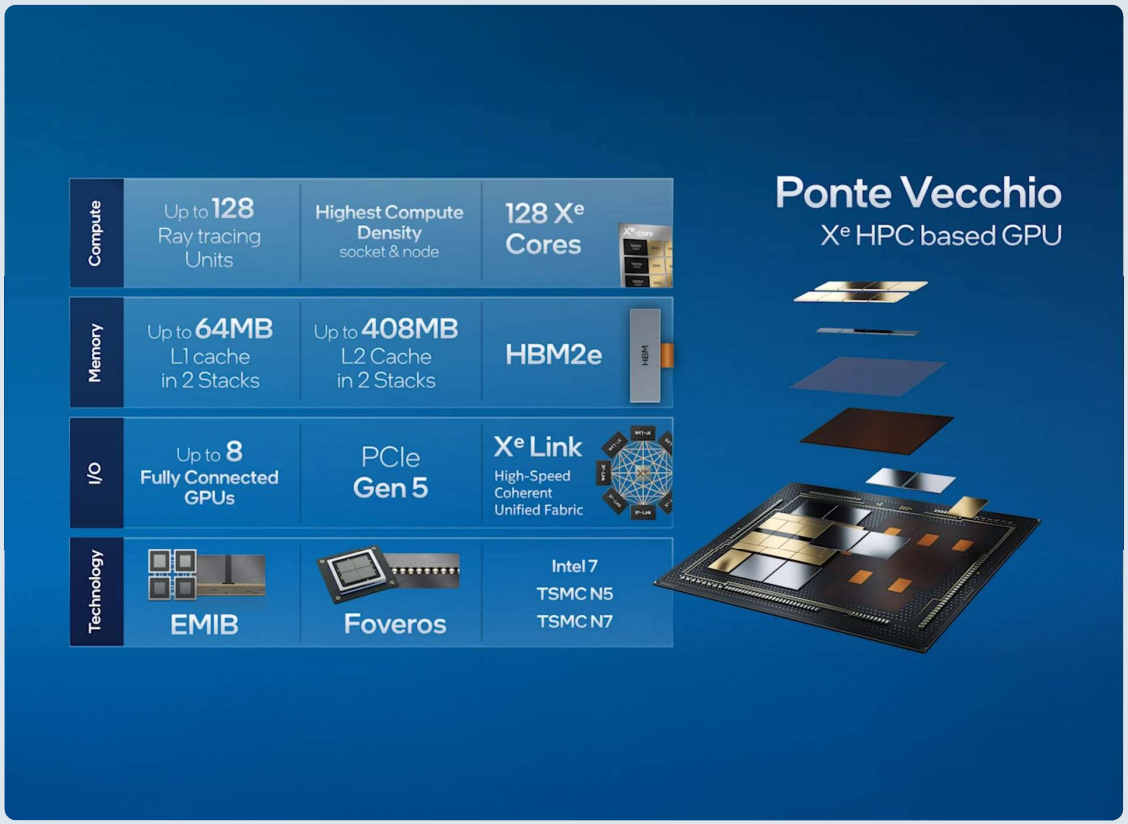


Die size scaling limited by reticle size and yield optimization



Semiconductor technology trend

Solution: die disaggregation and advanced packaging

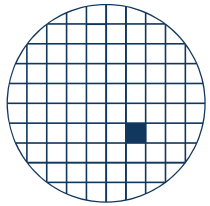


- Improved wafer-level yield with smaller chiplet
- Optimizing performance with mixed functionality capabilities
  - Memory
  - Co-packaged optics
- Allows for mixed technology node application and IP reuse

Source: Intel

Role of test in disaggregated world

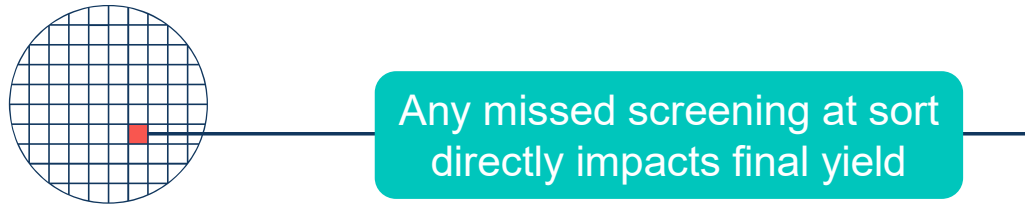
FRONT END		BACK END		
Wafer fabrication & pre-assembly preparation	**Wafer Testing Level**	Assembly	Packaging	**Final Testing Level**



Easy example: **single die** into a package

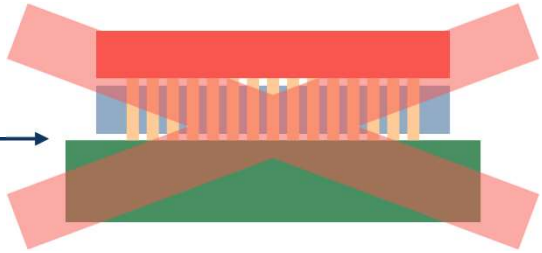
Role of test in disaggregated world

FRONT END		BACK END		
Wafer fabrication & pre-assembly preparation	**Wafer Testing Level**	Assembly	Packaging	**Final Testing Level**



Not good die

Any missed screening at sort directly impacts final yield



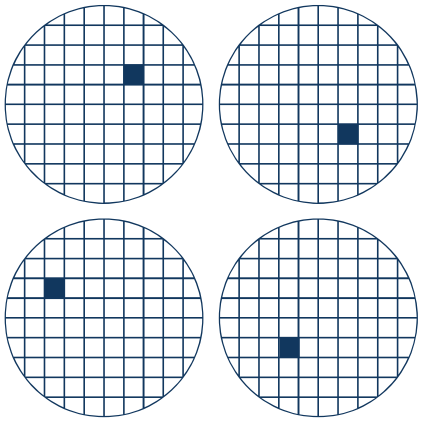
Cost of Front End coverage is balanced by relatively low substrate cost

Yield ~ HIGH

Assembly and packaging costs lost

Role of test in disaggregated world

FRONT END		BACK END		
Wafer fabrication & pre-assembly preparation	**Wafer Testing Level**	Assembly	Packaging	**Final Testing Level**

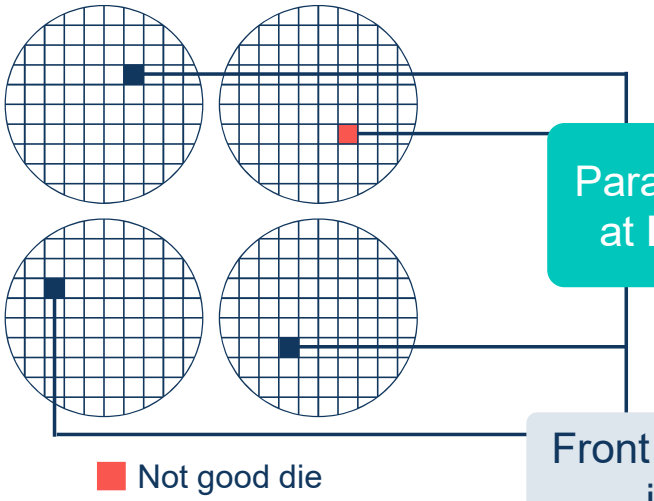


What about **four die**?

Role of test in disaggregated world

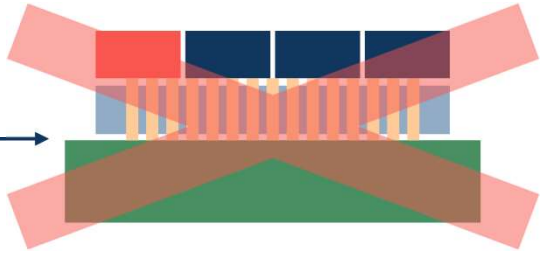
FRONT END | **BACK END**

Wafer fabrication & pre-assembly preparation	**Wafer Testing Level**	Assembly	Packaging	**Final Testing Level**



Paramount to screen at **Front End Test**

Front End Test coverage is more critical



Large Yield Impact

For each mis-screened die:
3 good die lost
- more wafer for each die
- still lose package

Advanced packaging vs standard

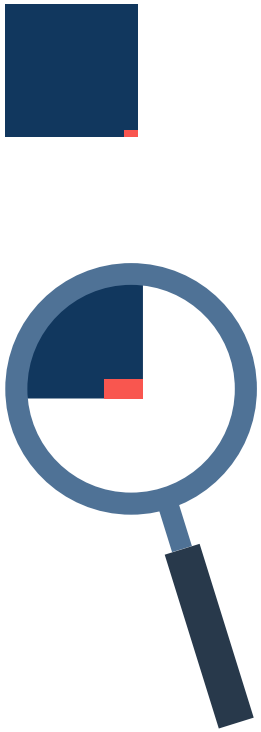
Standard

Manufacturing cost

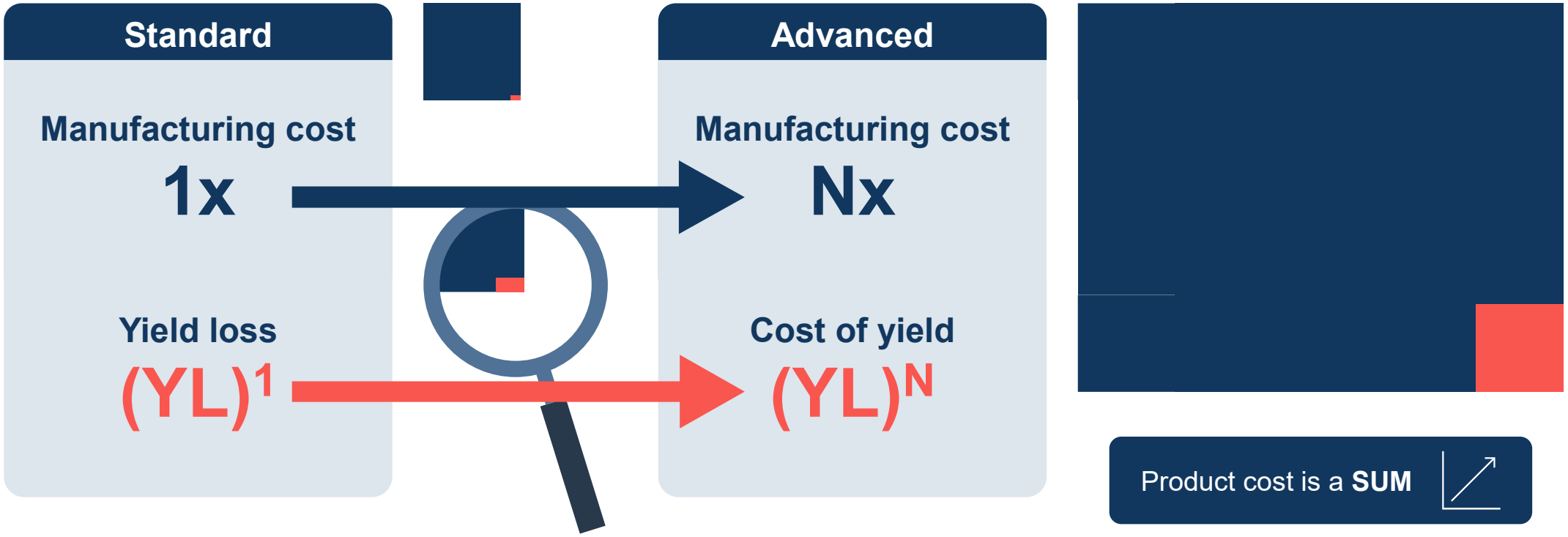
1x

Yield loss

(YL)[1]



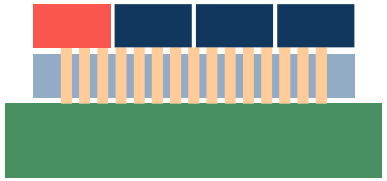
Advanced packaging vs standard



Product cost is a **SUM**

Cost of yield is NOT a sum but a **PRODUCT**

Role of test in disaggregated world

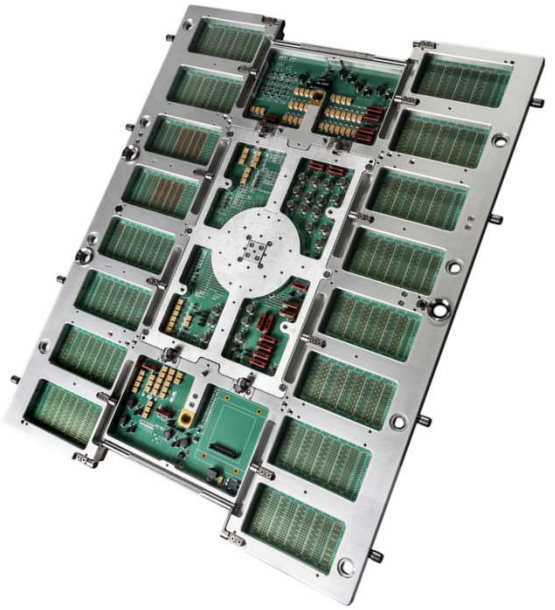


Front End Test coverage
is more critical

True **Known Good Die** required!

SOLUTION

more test at probe
=
more Probe Cards



Technoprobe as advanced packaging enabler

Fine pitch and ultra-large pin count

Necessary to effectively probe HPC and HBM's and all leading-edge product

High-speed

Short, ultra short and RF-specific needles technology to manage high speed interconnect IO, including SiPh

High power and thermal

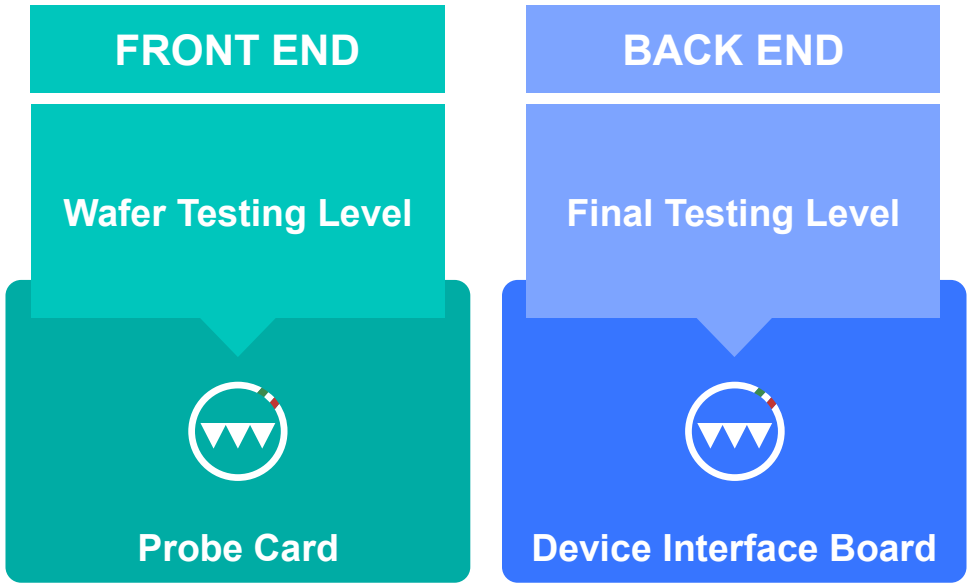
Delivering high power to DUT in effective and reliable way

Ability to remove heat dissipated by the probe card (directly or because of power transferred from DUT to PC)

High-density interconnect

Ultra-high complexity PCB and MLO/MLC for resource fan-out on ATE/SLT

Growth drivers & trajectories



Growth drivers & trajectories

FRONT END

Drive advancements in Logic Semiconductor Testing

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

Enter the High Bandwidth Memory (HBM) segment

BACK END

Strengthen positioning in Final Testing

Growth drivers & trajectories

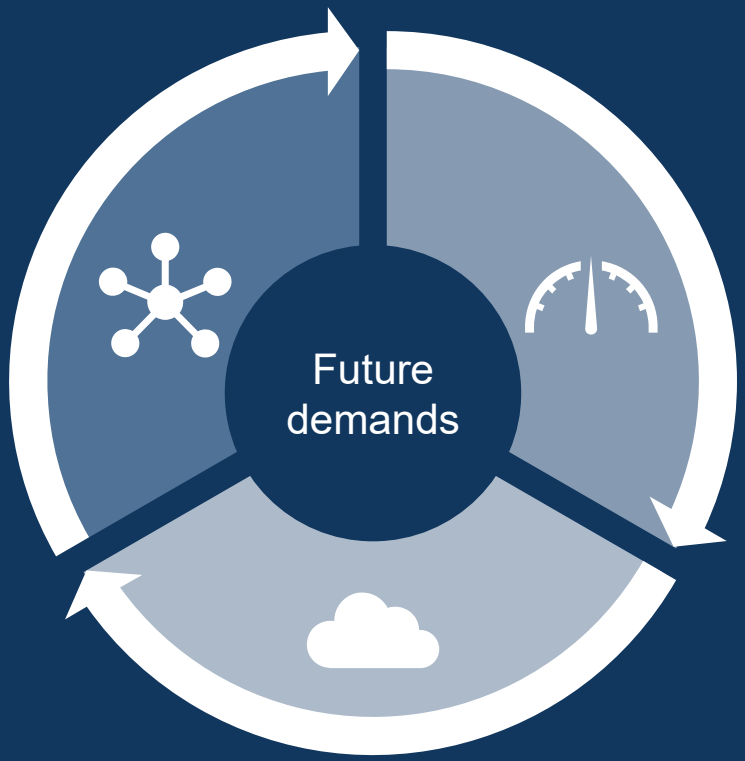
FRONT END

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Exponential increase in number & type of connected things



Bandwidth-hungry applications

Increasing reliance on the cloud

A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Exponential increase in number & type of connected things

Analog radio frequency

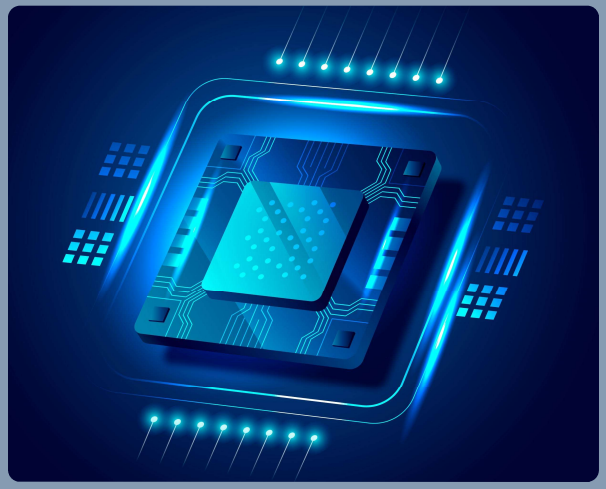
Satellite communications and sensing, automotive radar, mobile communication,…

A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Silicon photonics

Chiplet to chiplet interconnect
/ photonics-driven computing



A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Silicon photonics

Technoprobe technologies integrated in the same product enable…

Fine pitch probing	→	alignment with advanced packaging roadmap
Radio frequency probes	→	high-speed performances in same probe card solutions
Technoprobe IP	→	usage of standard wafer prober
Integration of other IP from specific segment suppliers	→	flexibility and compliancy with customer preferred test method

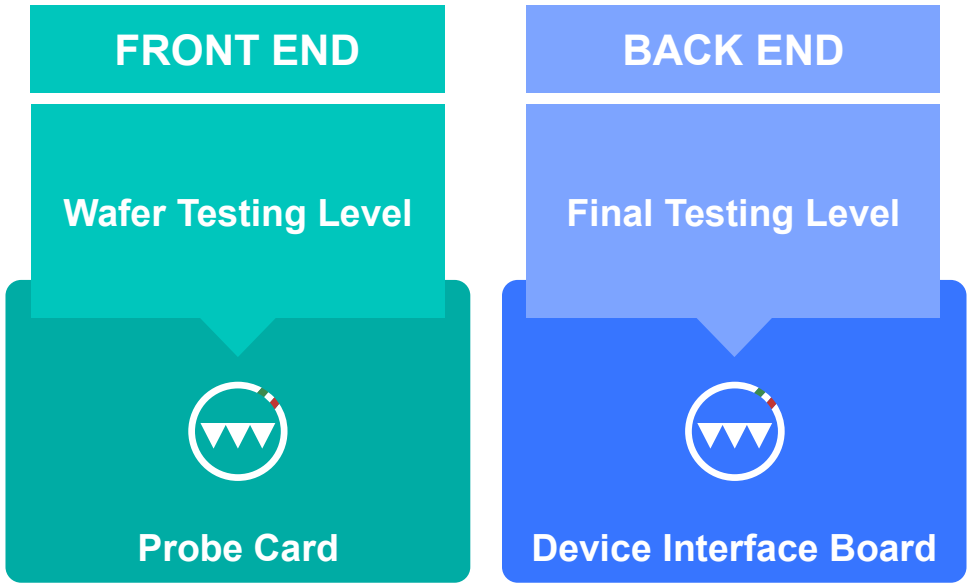
A hungry world of wideband applications

Future demands on the network will be driven by a combination of factors:

Chiplet probing

High density and high-speed IO inside chiplet demand for high-performance probe needles

Growth drivers & trajectories



Growth drivers & trajectories

FRONT END

Drive advancements in Logic Semiconductor Testing

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

Enter the High Bandwidth Memory (HBM) segment

BACK END

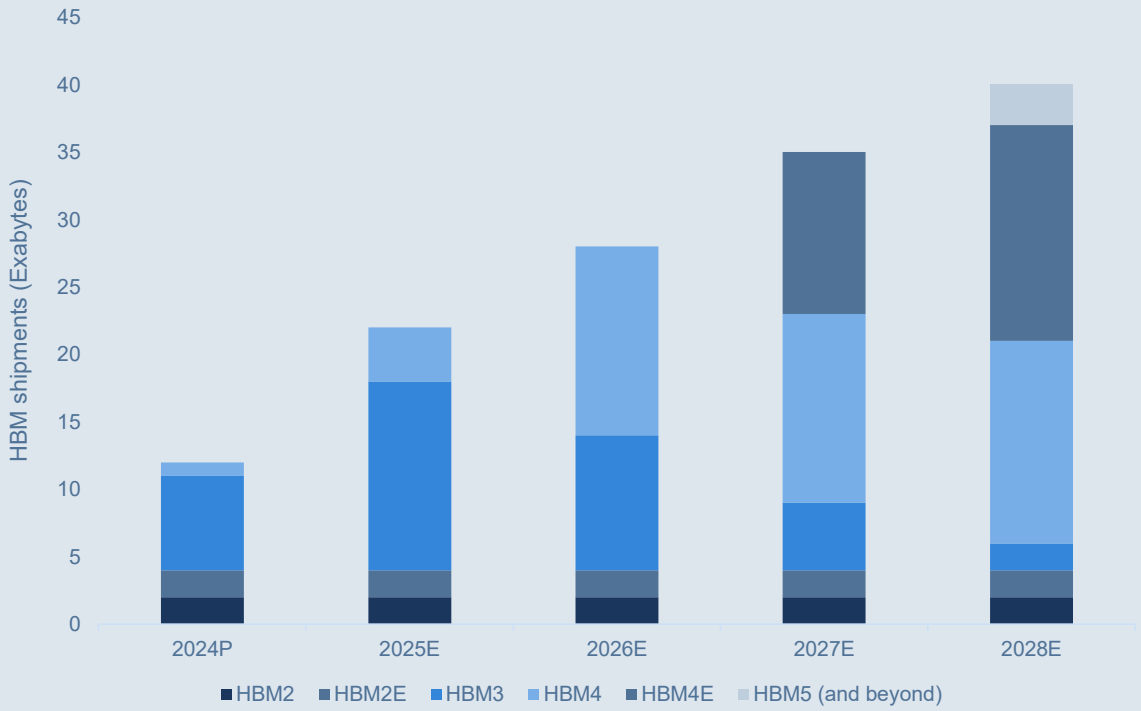
Strengthen positioning in Final Testing

Growth drivers & trajectories

FRONT END

Enter the High Bandwidth Memory (HBM) segment

DRAM & HBM: complexity as driver to new products



- **HBM demand continues to grow**
- **HBM bandwidth requirements almost double gen-gen**

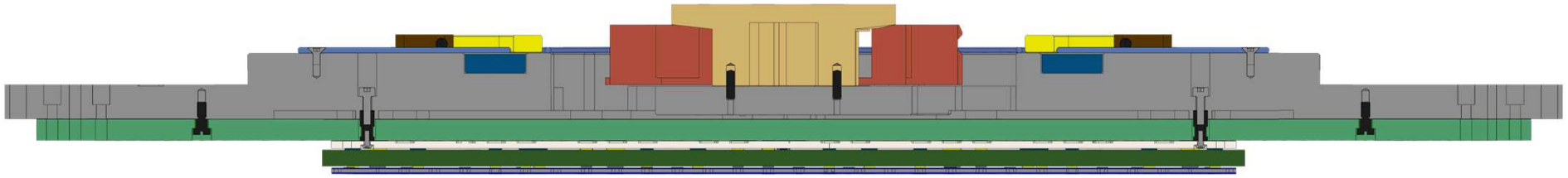
Source: Yole DRAM market monitor Q1 2025.

DRAM & HBM testing

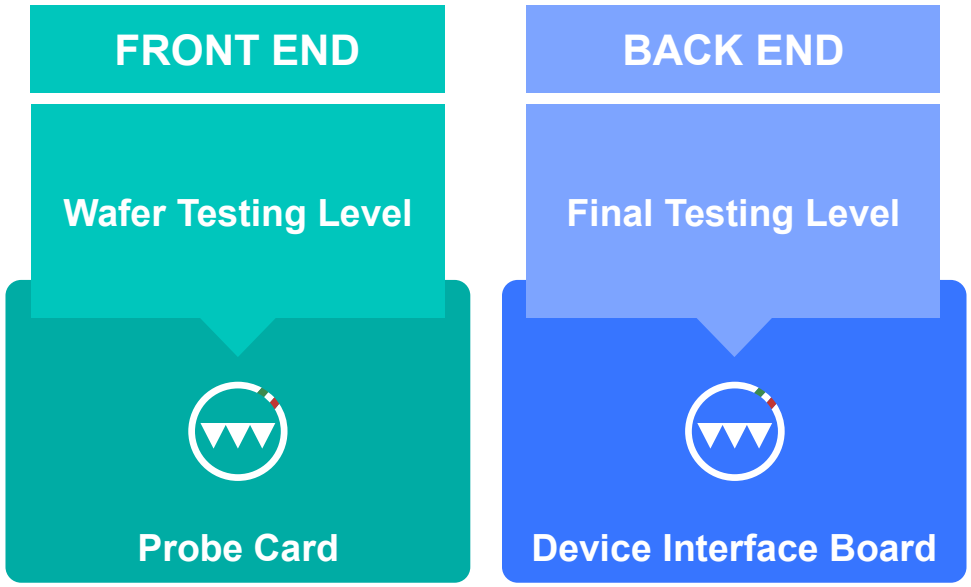
DRAM and HBM are typically tested with **microcantilever** probing technologies.

Most **advanced HBM** and Next Generation products are becoming more challenging in terms of pad pitch, signal integrity, and power.

For both applications Technoprobe is leveraging on **Vertical MEMS** solution and on a unique PC architecture.



Growth drivers & trajectories



Growth drivers & trajectories

FRONT END

Drive advancements in Logic Semiconductor Testing

Proliferate high-speed, high-voltage, radio frequency and silicon photonics

Enter the High Bandwidth Memory (HBM) segment

BACK END

Strengthen positioning in Final Testing

Growth drivers & trajectories

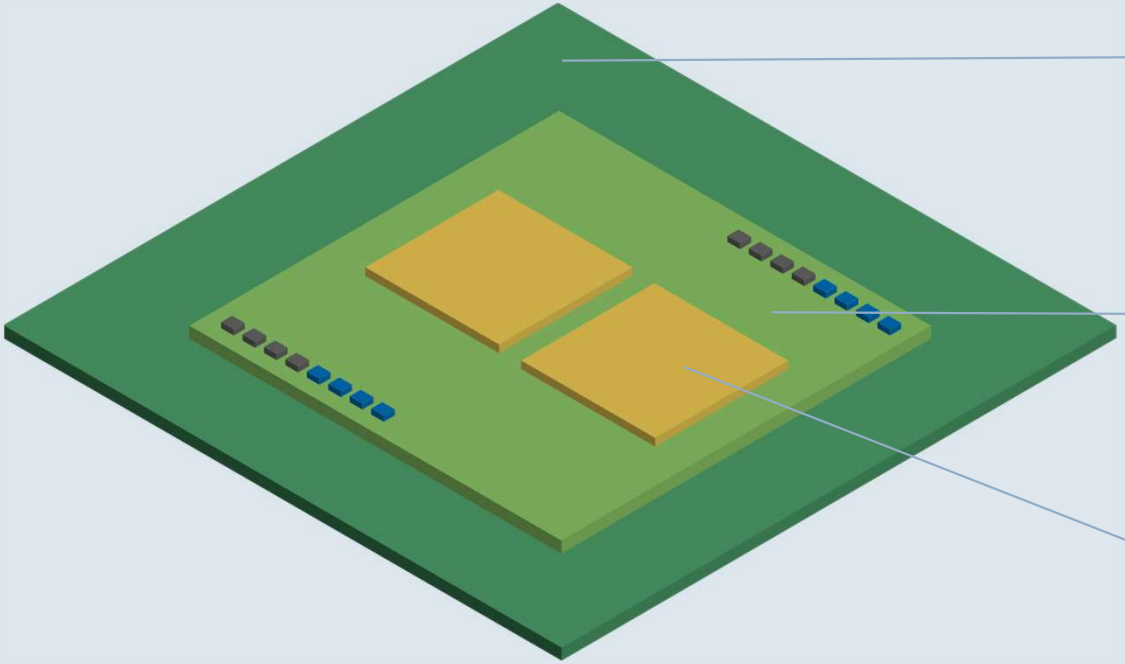
BACK END

Strengthen positioning in Final Testing

FusionLink

FUSIONLINK

We have applied the disaggregation to test interface hardware



Main motherboard
Best technology: printed circuit board (PCB)

Device substrate
Best technology: high density interconnect (HDI)

Probe substrate
Best technology: multi-layer organic (MLO)

Growth drivers & trajectories

FRONT END

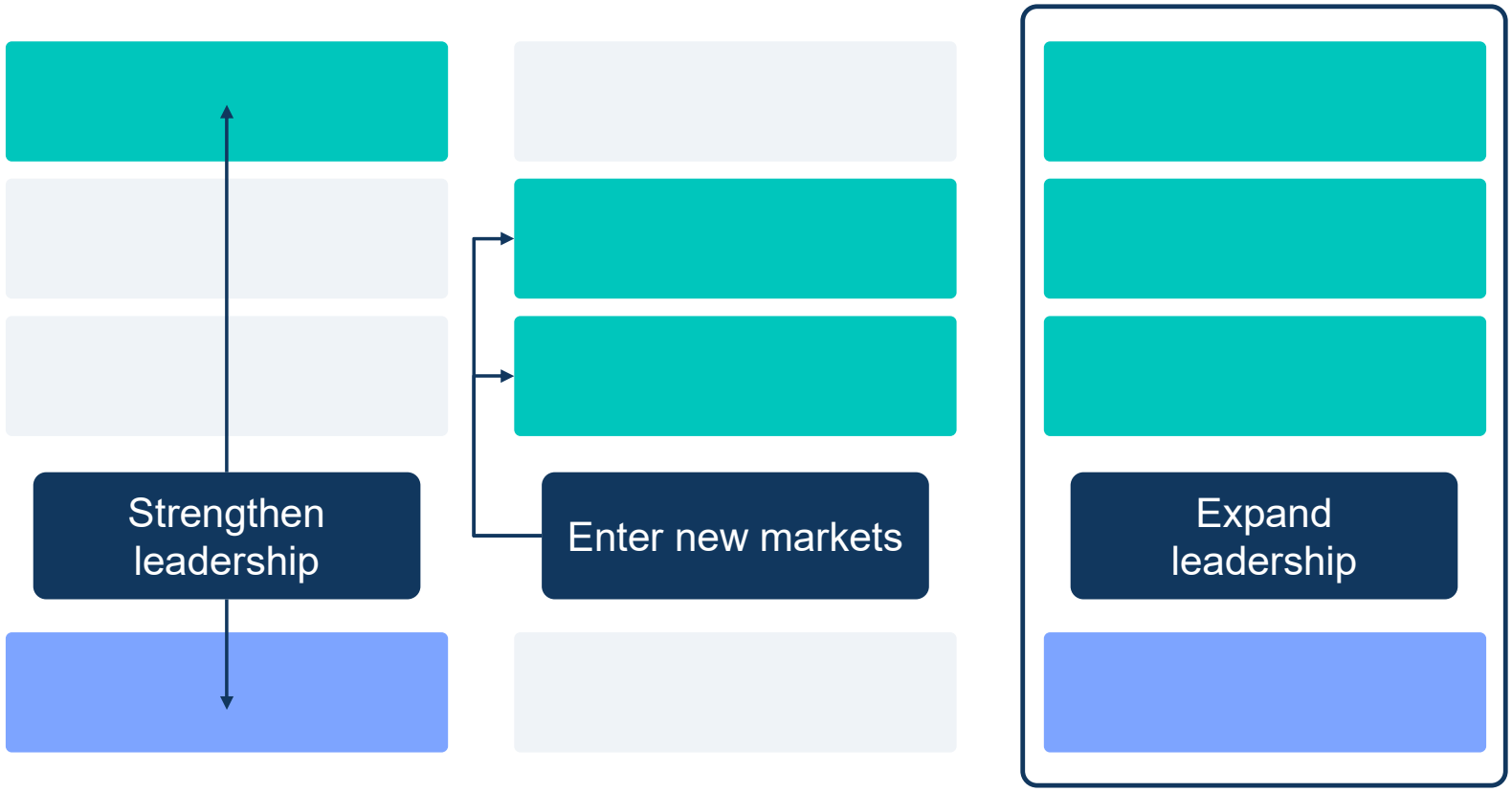
Advanced Packaging

Radio frequency & silicon photonics

HBM

BACK END

FusionLink



Agenda

Capital Market Day 2025

01 | **Our Vision & Strategy**
Stefano Felici - CEO

02 | **Market Perspective**
Marco Prea - CCO

03 | **Technology & Testing**
Joe Parks - CTO

04 | **Financial Outlook**
Stefano Beretta - CFO

Agenda

04 | **Financial Outlook**

Stefano Beretta - CFO

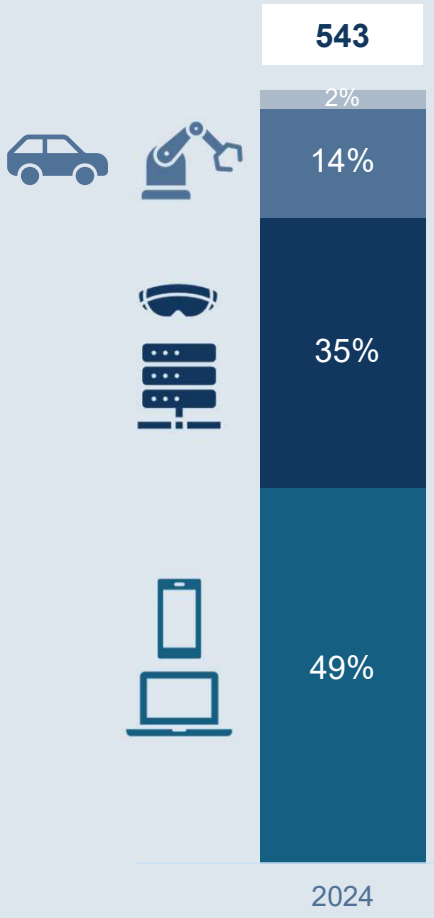
Capital Market Day 2025

Mid-terms scenario

1	**Technological complexity evolution**	→ Testing solution for Advanced Packaging → Increase in demand for high-precision tests
2	**Market trends**	→ AI will lead the growth for many market segments → Expansion of memory semiconductor segments
3	**Geo-political instability**	→ Technological sovereignty → Commercial policies

Market trends & revenues path

(€Mn)



2025 Growth

+ Low single digit

+ High double digit

+ Mid-single digit

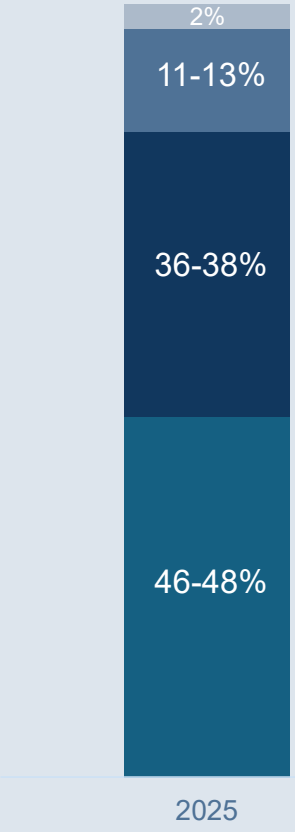
Market Assumptions

Destocking and inventory containment measures expected to remain sluggish

Expansion in volume for data center to continue strong demand growth expected

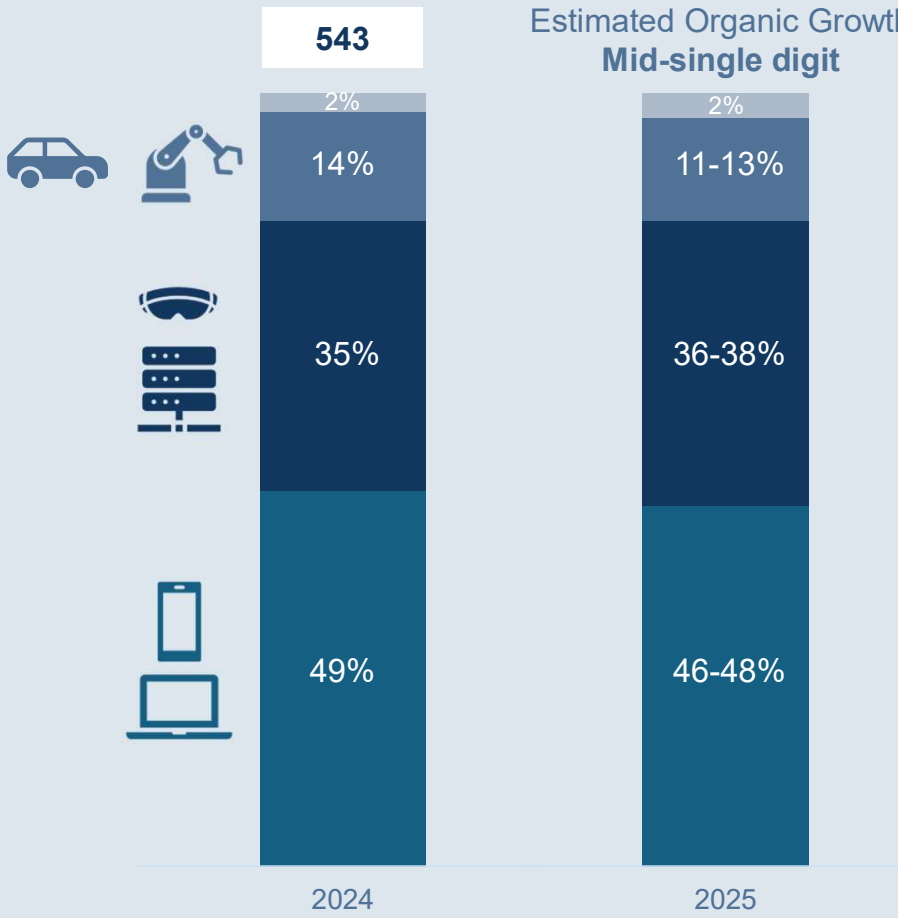
Volume stabilization / soft recovery
Waiting for Edge AI impact

Estimated Organic Growth:
Mid-single digit



Market trends & revenues path

(€Mn)

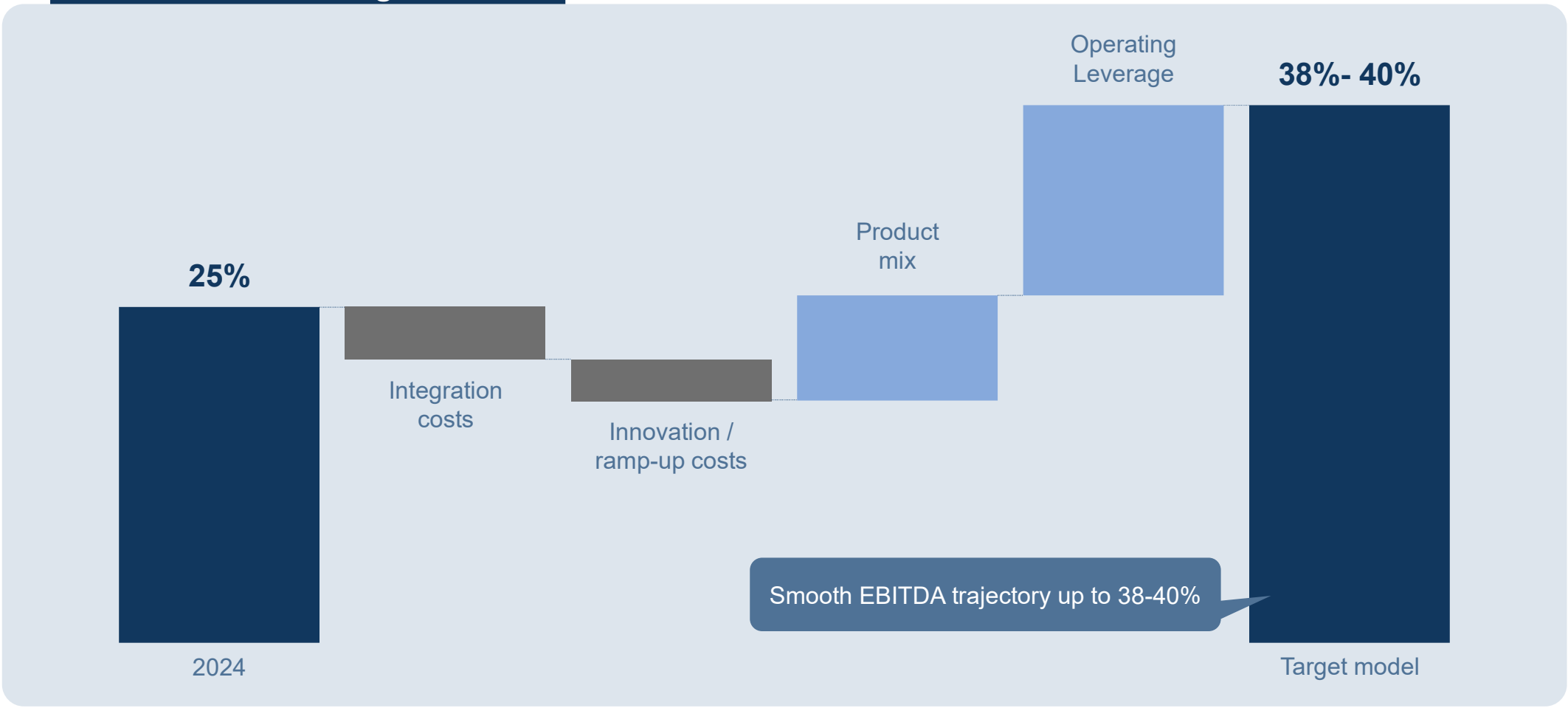


Market Assumptions

- Industry recovery
- Growth driven by data centers
- Positive impact of Edge AI

Profitability profile

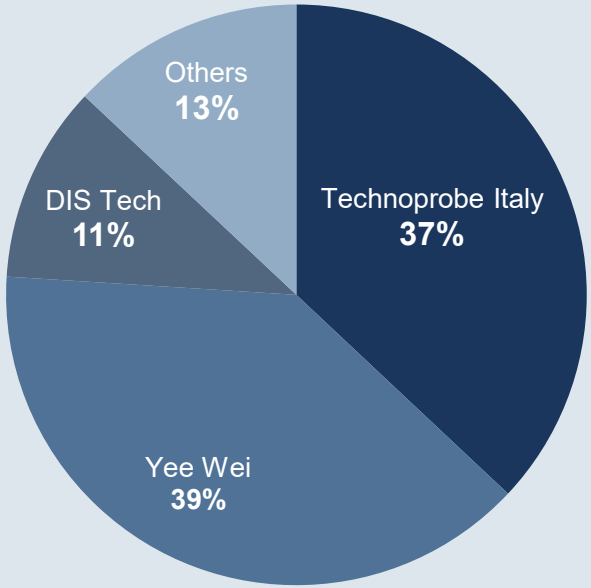
EBITDA margin



Capex

(€Mn)

FY 2024



	FY 2022	FY 2023	FY 2024	Target Model
Revenues	549	409	543	
Capex	84	73	100	
Capex as % of Revenues	*15%*	*18%*	*18%*	*8% - 10%*

Q&A