Challenges probing next generation full array products with 60 µm pitch and below

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Co-authors: Erik Jan Marinissen – IMEC
Jerry Broz – ITS
Overview

- Background
- Next generation device trend and requirements
  - Probe card and probing challenges
- Technoprobe probing solutions at 60 µm pitch and below
  - Technology evolution – a few case studies: μ-Cu pillars
  - On-going tests at IMEC on WIDE I/O2 down to 40 µm pitch
- On-line cleaning process optimization
  - On-line cleaning sheet mechanical benchmark with ITS
- Space transformer challenges and roadmap
- Conclusions and future work
Background

• Over the last 3-4 years, the requirements of probing dense arrays of bumps have been more and more demanding

• To address our customers needs we have been developing new approaches in probing and space transformer technologies (presented at SWTW 2013-14) introducing:
  – TPEG™ MEMS T3, to overcome all limitations of previous Cobra-like technologies (SWTW 2013)
  – TPEG™ MEMS T1, to allow probe on μ-Cu pillar bumps (SWTW 2014)

• Furthermore, understanding the overall industry needs is a critical step to translate our customers’ next generation challenges in probe cards evolution
Next generation device trend and requirements

Systems scaling as a new frontier

• Last 50 Years
  – Transistor scaling with minimum focus on system miniaturization

• Next 50 Years
  – System scaling in conjunction with Transistor scaling
  – System scaling for Mobile devices
Next generation devices trends and requirements

Probes card challenges

- **Pitch reduction trends**
  - Mobile processors → 80 um
  - HBM → 50 um
  - Wide I/O → 40 um
  - Mixed pitch & current
  - PH technology scalability is key as well as the development of advanced space transformers

- **Electrical yield**
  - C_RES stability
  - Functional tests: low probe R required
  - Current capability: low resistivity materials needed
  - High speed tests: special probes and layout must be designed
  - Probes and PH design must be tailored to Customer applications: specific PH mechanics, advanced probe alloys, special probe designs must be developed

SoC (MPU) Bump pitch Roadmap changes over time

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Probe card concept evolution
From simple interface to system level approach

- Continuous pitch reduction
- SI/PI optimization
- Customized probes
- Customized mechanics
- Advanced probers and prober setups
- Complex docking systems
- Advanced testing

Scalability limited by ST availability
Scalability limited by probes development
Probe card as a system to be integrated in complex probing environment

Min pitch: 130 um → 110 um → 90 um → 80 um → 60 um → 40 um

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SW Test Workshop
A few case studies are presented to give an overview of how important it is to adopt a system level approach:
- probe alloy, probe design, PH mechanics, probing setup and customer product peculiarities must be considered since the beginning

Case studies:
- CASE 1: TPEG™ MEMS T60 developed for next generation microprocessors at 60 µm pitch (25 µm ∅ μCu pillar bumps). Results on Customer test wafers.
- CASE 2: Vertical FT1 developed for 40 µm pitch μbump direct probing. Joint tests with IMEC and TEL.
Case 1: Direct μ-bumps probing @ 60 µm pitch
Customer requirements – TP probing solution

• **Target:** define and qualify a robust probing technology to test next generation microprocessors
  - Min pitch: 60 µm
  - μ- Cu pillars with solder cap: 25 µm diameter
  - Maximum bump damage less than 30% of the area
  - Stable CGRESS

• **TP solution:** low force TPEG™ MEMS T60
  - Next slides are showing the results of TP investigation on test wafers comparing the scrub area and C_RES performances depending on probe force, PH mechanics and on probe alloy
  - First step: probe force and PH mechanics optimization to match bump damage requirements even in the worst case (max OD – 6 consecutive TDs)
  - Second step: probe alloy and probe tip design & shape optimization to get stable C_RES
Case 1: T60 for μ-bumps direct probing
Probe force and mechanics optimization

- Force & Alignment must be controlled to have reduced pillar cap damage
  - Probe force and probe mechanics optimization using as reference TPEG™ MEMS T1 today already in mass production @ 80 μm pitch

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Case 1: T60 for µ-bumps direct probing

**C_RES tests setup**

- **C_RES TESTS SETUP on Customer TV wfs**
  - A few C_RES pairs available (in short @ wafer top metal level)

- **Measurement principle: Force V – Measure I**
  - Force V = 10 mV
  - Clamp I = 50 mA
  - $R \text{ Pair} = 0.5 \times \frac{V}{I}$
Case 1: T60 for μ-bumps direct probing
Probes fine tuning for optimal C_RES stability

- **TPEG™ MEMS T60 probes and probe head mechanics have been specifically fine tuned to guarantee stable C_RES even with reduced probing force**
  - A new probe alloy has been specifically developed (Alloy C)
  - Below box plot is showing the results obtained, with respect to TPEG™ MEMS T1 that is today in mass production down to 80 µm pitch

![Box plot showing CRES values for different conditions](image)
Case 2: 40 µm pitch direct µbump probing
IMEC – Technoprobe - TEL

- **Imec’s Blanket Micro-Bump (BMB) Design**
  - Includes JEDEC WIO2 foot-print (40 µm pitch)
  - Micro-bumps: Ø 25 µm Cu and Ø 15 µm Cu/Ni/Sn

- **Technoprobe’s Probe Technology**
  - FT1.0 vertical needles, micro-wired space transformer
  - Probe card with single-bank WIO2

- **Test Equipment @ imec**
  - TEL P-12XLM automatic probe station
  - Agilent 4073 parametric tester

- **Evaluation Criteria**
  - Contact resistance (C_RES)
  - Probe marks
Case 2: 40 µm pitch direct µbump probing
Blanket Micro-Bump Wafers

- Ø 25µm Cu
- (10nm NiB coating)

- Ø 15µm Cu/Ni/Sn
Case 2: 40 µm pitch direct µbump probing
Initial results with pointed tips

• Preliminary C_RES results with pointed tips are summarized here below.

• Pointed Tips, OT=75µm - Mean C_RES
  – Overall: 30.97 Ω
  – Zero dummy rings : 28.49 Ω
  – One dummy ring : 31.04 Ω
  – Two dummy rings : 33.38 Ω

• Pointed Tips, OT=85μm - Mean C_RES
  – Overall: 27.69 Ω
  – Zero dummy rings : 26.19 Ω
  – One dummy ring : 28.69 Ω
  – Two dummy rings : 28.18 Ω
Case 2: 40 µm pitch direct µbump probing

Initial results with flat tips

• First results with flat tips are reported below

D02: Cu+NiB
- \( C_{RES} \) remains in range 4-50 Ω
- Mean* \( C_{RES} = 28.39 \) Ω
- Cu even harder to probe due to NiB

D03: Cu
- \( C_{RES} \) remains in range 4-50 Ω
- Mean* \( C_{RES} = 17.20 \) Ω

D04: Cu/Ni/Sn
- \( C_{RES} \) remains largely in range 4-6 Ω
- Mean* \( C_{RES} = 4.44 \) Ω
- Sn is a lot easier to probe than Cu

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On-line cleaning optimization with ITS
Target and test methodology adopted

• A typical example of strong partnership with a key Supplier of our Customers is reported

• Case study: on-line cleaning wear-out optimization in cooperation with International Test Solutions is reported (ITS – Jerry Broz)
  – Target: reduce on-line cleaning wear out rate for both TPEG™ MEMS T3 and T1 used in probing high volumes Cu pillars and µ-bumps
  – Test methodology: benchmarking
On-line cleaning optimization with ITS Benchmark description

- **Benchmark is based on:**
  - Confocal imaging (50x, \(\sim 0.5 \text{ mm} \times 0.5 \text{ mm} \) area) : see below
  - Tip consumption (wear rate) and tip finishing : see next slides

<table>
<thead>
<tr>
<th>3M-3µm 266x - Nominal grit 3µm (Al2O3)</th>
<th>ITS PL 1AH - Nominal grit 1µm (Al2O3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ra (~1.1 - 1.4 \mu m)</td>
<td>Ra (~1.9 - 2.1 \mu m)</td>
</tr>
<tr>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ITS PL 1SH - Nominal grit 1µm (SiC)</th>
<th>ITS PL 3SH - Nominal grit 1µm (SiC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ra (~1.3 - 1.4 \mu m)</td>
<td>Ra (~1.7 - 2.1 \mu m)</td>
</tr>
<tr>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
</tr>
</tbody>
</table>
On-line cleaning optimization with ITS
Summary of wear out data

- No major tip surface finishing differences have been detected
- With respect to 3M 3µm, ITS PL cleaning media show lower wear rates: PL 1SH is the most promising one

<table>
<thead>
<tr>
<th>Technology</th>
<th>Cleaning media</th>
<th>Cleaning movement</th>
<th>Wear-out rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPEG™ MEMS T1</td>
<td>3M-3µm</td>
<td>X-Y</td>
<td>Ref.</td>
</tr>
<tr>
<td></td>
<td>PL 1AH</td>
<td>X-Y</td>
<td>-10%</td>
</tr>
<tr>
<td></td>
<td>PL 1SH</td>
<td>X-Y</td>
<td>-20%</td>
</tr>
<tr>
<td></td>
<td>PL 3SH</td>
<td>X-Y</td>
<td>0%</td>
</tr>
</tbody>
</table>
## On-line cleaning optimization with ITS Tip finishing

<table>
<thead>
<tr>
<th>Technology</th>
<th>Cleaning media</th>
<th>Tip image</th>
<th>Tip Ra [µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPEG™ MEMS T1</td>
<td>3M-3µm</td>
<td><img src="image1.png" alt="Tip image" /></td>
<td>~ 500 nm</td>
</tr>
<tr>
<td></td>
<td>PL 1AH</td>
<td><img src="image2.png" alt="Tip image" /></td>
<td>~ 490 nm</td>
</tr>
<tr>
<td></td>
<td>PL 1SH</td>
<td><img src="image3.png" alt="Tip image" /></td>
<td>~ 400 nm</td>
</tr>
<tr>
<td></td>
<td>PL 3SH</td>
<td><img src="image4.png" alt="Tip image" /></td>
<td>~ 510 nm</td>
</tr>
</tbody>
</table>
We are now facing a new paradigm: probe card scalability is not limited by probes but more and more by space transformer availability.

Below 80 µm pitch only few MLO and/or MLC suppliers are providing working solutions with increasing costs and delivery times.

Next slide is summarizing today Technoprobe capability and roadmap down to 40 µm pitch.
Technoprobe developed a dedicated supply chain for MLO/MLC interconnections, in order to cover the broadest range possible of required probe depths and layout/pitch configurations.

**Standard solution:**
- Wired and μ-wired ST (40um pitch min)

**ROADMAP**
- Micro organic interposer (60um pitch) - In qualification phase, Availability eJune’15
- U-fine pitch MLC (50um pitch) - Available
- Micro Interposer (40um pitch) - In qualification phase, Availability eJune’15
## Space transformer
### Solutions available @ TP

<table>
<thead>
<tr>
<th>ST technology</th>
<th>Image/sketch</th>
<th>Min pitch</th>
<th>Status</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro Organic Interposer</td>
<td><img src="image1.png" alt="Image" /></td>
<td>50 µm</td>
<td>eJune’15</td>
<td>Build up: 3(5) layers L/S 6/6 µm Core: 2 layers vias pitch 110 µm</td>
</tr>
<tr>
<td>U-fine pitch MLC</td>
<td><img src="image2.png" alt="Image" /></td>
<td>60 µm</td>
<td>Available</td>
<td>Build up: 4 layers L/S 10/10 µm Core: 2 layers vias pitch 110 µm</td>
</tr>
<tr>
<td>Silicon Interposer</td>
<td><img src="image3.png" alt="Image" /></td>
<td>40 µm</td>
<td>eJune’15</td>
<td>TSV diameter 10µm TSV pitch 40µm L/S 5/5µm</td>
</tr>
</tbody>
</table>

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**SW Test Workshop**
When probing at 40 µm pitch is concerned, only micro-interposer solution can be used.

50 by 50 mm² Interposers successfully soldered and tested on test PCBs:
- 10 um co-planarity achieved
- Fully electrical functionality achieved

- TSV diameter 10um
- TSV pitch 40um
- Trace width/gap 5/5um

- Full probe card assembled and tested successfully @ t₀
Conclusions

• We are in front of a two fold, huge change of probe card paradigms:
  – Probe cards moved from just an electro-mechanical interface to a system, to be integrated in a high complexity probing environment
  – More recently probe card scalability is moving from probes/probe head limitations to space transformer availability limitations

• Win/win strong partnerships are needed between main Suppliers and Customers to have full visibility of evolving requirements and full control of the design and manufacturing of most critical probe card components.

• The presentation gave you a quick overview of how Technoprobe is working to achieve this target
Future work

On-going developments down to 40 µm pitch

• Further developments are on-going to define the best possible probing solution to probe over μ-pads and μ-Cu pillars down to 40 µm pitch full array

• TPEG™ MEMS T40, recently introduced, will be tested within the cooperation frame between IMEC, Technoprobe and TEL
Thank you!

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